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Electromagnetic compatibility and Radio spectrum Matters (ERM); Digital Mobile Radio (DMR) Systems; Part 1: DMR Air Interface (AI) protocol

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Contents

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Foreword

This Technical Specification (TS) has been produced by ETSI Technical Committee Electromagnetic compatibility and Radio spectrum Matters (ERM).

The present document is part 1 of a multi-part deliverable covering the Technical Requirements for Digital Mobile Radio (DMR), as identified below:

Part 1: "DMR Air Interface (AI) protocol";

Part 2: "DMR voice and generic services and facilities";

Part 3: "DMR data protocol";

Part 4: "DMR trunking protocol".

Modal verbs terminology

In the present document "**shall**", "**shall not**", "**should**", "**should not**", "**may**", "**need not**", "**will**", "**will not**", "**can**" and "**cannot**" are to be interpreted as described in clause 3.2 of the ETSI Drafting Rules (Verbal forms for the expression of provisions).

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1 Scope

The present document contains technical requirements for Digital Mobile Radio (DMR) operating in the existing licensed land mobile service frequency bands, as identified in CEPT/ERC/T/R 25-08 [i.3].

The present document describes the Air Interface of a scalable Digital Mobile Radio system which covers three tiers of possible products:

- Tier I: DMR equipment having an integral antenna and working in direct mode (communication without infrastructure) under a general authorization with no individual rights operation.
- Tier II: DMR systems operating under individual licences working in direct mode or using a Base Station (BS) for repeating.
- Tier III: DMR trunking systems under individual licences operating with a controller function that automatically regulates the communications.

NOTE 1: Tier II and Tier III products encompass both simulcast and non-simulcast systems.

NOTE 2: The three tiers of possible products will work only independently and not interoperable.

(For more information please see the System reference documents ETSI TR 102 335-1 [i.1] and ETSI TR 10 335 2 [i.2].)

The present document specifies the Air Interface, complying with either ETSI EN 300 113-1 [1] and ETSI EN 300 113-2 [2] or ETSI EN 300 390-1 [3] and ETSI EN 300 390-2 [4], that has been specifically developed with the intention of being suitable for all identified product tiers. A polite spectrum access protocol for sharing the physical channel has also been specified. Specifically, in this case for use in the existing land mobile service bands with the intention of causing minimum change to the spectrum planning and regulations. Thus the DMR protocol is intended to be applicable to the land mobile frequency bands, physical channel offset, duplex spacing, range assumptions and all other spectrum parameters without need for any change.

2 References

2.1 Normative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the reference document (including any amendments) applies.

Referenced documents which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

NOTE: While any hyperlinks included in this clause were valid at the time of publication, ETSI cannot guarantee their long term validity.

The following referenced documents are necessary for the application of the present document.

[1] ETSI EN 300 113-1: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Land mobile service; Radio equipment intended for the transmission of data (and/or speech) using constant or non-constant envelope modulation and having an antenna connector; Part 1: Technical characteristics and methods of measurement".

[2] ETSI EN 300 113-2: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Land mobile service; Radio equipment intended for the transmission of data (and/or speech) using constant or non-constant envelope modulation and having an antenna connector; Part 2: Harmonized EN covering the essential requirements of article 3.2 of the R&TTE Directive".

[3] ETSI EN 300 390-1: "ElectroMagnetic Compatibility and Radio Spectrum Matters (ERM); Land Mobile Service; Radio equipment intended for the transmission of data (and speech) and using an integral antenna; Part 1: Technical characteristics and test conditions".

[4] ETSI EN 300 390-2: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Land Mobile Service; Radio equipment intended for the transmission of data (and speech) and using an integral antenna; Part 2: Harmonized EN covering essential requirements under article 3.2 of the R&TTE Directive".

[5] ETSI TS 102 361-2: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Digital Mobile Radio (DMR) Systems; Part 2: DMR voice and generic services and facilities".

[6] IETF RFC 791: "Internet Protocol; DARPA Internet Program; Protocol Specification".

[7] Void.

[8] IEC 61162-1: "Maritime navigation and radiocommunication equipment and systems - Digital interfaces - Part 1: Single talker and multiple listeners".

[9] ISO/IEC 646: "Information technology -- ISO 7-bit coded character set for information interchange".

[10] ISO/IEC 8859: "Information technology -- 8-bit single-byte coded graphic character sets".

[11] ETSI TS 102 361-4: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Digital Mobile Radio (DMR) Systems; Part 4: DMR trunking protocol".

[12] ETSI TS 102 361-3: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Digital Mobile Radio (DMR) Systems; Part 3: DMR data protocol".

2.2 Informative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the reference document (including any amendments) applies.

NOTE: While any hyperlinks included in this clause were valid at the time of publication, ETSI cannot guarantee their long term validity.

The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

[i.1] ETSI TR 102 335-1: "Electromagnetic compatibility and Radio spectrum Matters (ERM); System reference document for harmonized use of Digital Mobile Radio (DMR); Part 1: Tier 1 DMR#, expected to be for general authorization with no individual rights operation".

[i.2] ETSI TR 102 335-2: "Electromagnetic compatibility and Radio spectrum Matters (ERM); System reference document for harmonized use of Digital Mobile Radio (DMR); Part 2: Systems operating under individual licences in the existing land mobile service spectrum bands".

[i.3] CEPT/ERC/T/R 25-08: "Planning criteria and co-ordination of frequencies in the Land Mobile Service in the range 29,7 - 921 MHz".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

1:1-mode: 1 traffic channel mode

NOTE: 1:1-mode supports one "MS to fixed end" duplex call or one simplex call with an optional inbound RC using a two frequency BS.

2:1-mode: 2 traffic channel mode

NOTE: 2:1-mode supports two independent calls which may be either "MS to fixed end" duplex calls, simplex calls using a two frequency BS or simplex calls between MS units on a single frequency.

backward: logical channel from target to source in direct mode

Base Station (BS): fixed end equipment that is used to obtain DMR services

bearer service: telecommunication service providing the capability for information transfer between access points

burst: elementary amount of bits within the physical channel

NOTE 1: Three different bursts exist with different number of bits. The Traffic burst contains 264 bits, the CACH burst contains 24 bits and the RC burst contains 96 bits.

NOTE 2: The burst may include a guard time at the beginning and end of the burst used for power ramp-up and ramp-down.

NOTE 3: For detailed burst definition see clause 4.2.1.

call: complete sequence of related transactions between MSs

NOTE: Transactions may be one or more bursts containing specific call related information.

channel slot timing: time slot 1 and time slot 2 timing boundaries established by a TDMA direct mode leader

Control plane (C-plane): part of the DMR protocol stack dedicated to control and data services

conventional: non-trunked communication

NOTE: This is a communication technique where any radio unit (MS) may communicate with one or more other radio units (MSs) without using a trunking protocol, and may be either in direct mode or using any additional equipment (e.g. BS).

Digital Mobile Radio (DMR): physical grouping that contains all of the mobile and/or fixed end equipment that is used to obtain DMR services

direct mode: mode of operation where MSs may communicate outside the control of a network

NOTE 1: This is communication technique where any radio unit (MS) may communicate with one or more other radio units (MSs) without the need for any additional equipment (e.g. BS).

NOTE 2: Supports one transmission per 12,5 kHz frequency; 12,5 kHz equivalent (12,5e) spectral efficiency.

duplex: mode of operation by which information can be transferred in both directions and where the two directions are independent

NOTE: Duplex is also known as full duplex.

forward: logical channel from source to target in direct mode

frame: two contiguous time slots labelled 1 and 2

NOTE: A frame has a length of 60 ms.

Golay code: type of error correcting code named Golay

Hamming code: type of error correcting code named Hamming

inbound: MS to BS transmission

logical channel: distinct data path between logical endpoints

NOTE: The logical channels are labelled 1 and 2. The logical channel may consist of sub-channels, e.g. SYNC, embedded signalling, etc.

Mobile Station (MS): physical grouping that contains all of the mobile equipment that is used to obtain DMR mobile services

outbound: BS to MS transmission

payload: bits in the information field

physical channel: RF carrier that is modulated with information bits of the bursts

NOTE: The RF carrier may be a single frequency or a duplex pair of frequencies. The physical channel of a DMR subsystem is required to support the logical channels.

polite protocol: "Listen Before Transmit" (LBT) protocol

NOTE: This is a medium access protocol that implements a LBT function in order to ensure that the channel is free before transmitting.

privacy: secret transformation

NOTE: Any transformation of transmitted information that is derived from a shared secret between the sender and receiver.

Protocol Data Unit (PDU): unit of information consisting of protocol control information (signalling) and possibly user data exchanged between peer protocol layer entities

Radio Frequency channel: radio frequency carrier (RF carrier)

NOTE: This is a specified portion of the RF spectrum. In DMR, the RF carrier separation is 12,5 kHz. The physical channel may be a single frequency or a duplex spaced pair of frequencies.

Received Signal Strength Indication (RSSI): root mean squared (rms) value of the signal received at the receiver antenna

Reed-Solomon code: type of error correcting code named Reed-Solomon

repeater mode: mode of operation where MSs may communicate through a BS

NOTE: This is a communication technique where any radio unit (MS) may communicate with one or more other radio units (MSs) with the need for an intermediate BS.

Reverse Channel (RC): signalling burst from target to source

signalling: exchange of information specifically concerned with the establishment and control of connections, and with management, in a telecommunication network

simplex: mode of working by which information can be transferred in both directions but not at the same time

superframe: 6 continuous traffic bursts on a logical channel labelled "A" to "F"

NOTE: A superframe has a length of 360 ms and is used for voice traffic only.

TDMA direct mode: direct mode operation that supports two transmissions per 12,5 kHz frequency

NOTE: Supports 6,25 kHz equivalent (6,25e) spectral efficiency.

time slot (or slot): elementary timing of the physical channel

NOTE: A timeslot has a length of 30 ms and will be numbered "1" or "2".

transmission: transfer period of bursts containing information or signalling

NOTE: The transmission may be continuous, i.e. multiple bursts transmission without ramp-up, ramp-down, or discontinuous, i.e. single burst transmission with ramp-up and ramp-down period.

Trellis code: type of error correcting code for modulation named Trellis

trunking: network controlled communication

NOTE: This is a communication technique where any radio unit (MS) may communicate with one or more other radio units (MSs) using a trunking protocol and all MSs will be under control of a network.

User plane (U-plane): part of the DMR protocol stack dedicated to user voice services

vocoder socket: 216 bits vocoder payload

3.2 Symbols

For the purposes of the present document, the following symbols apply:

dBm	absolute power level relative to 1 mW, expressed in dB
dBp	Power relative to the average power transmitted over a burst in decibel
Dibit	2 bits grouped together to represent a 4-level symbol
Eb	Energy per bit
Nibble	4 bits grouped together
No	Noise per Hz
Octet	8 bits grouped together, also called a byte
Tribit	3 bits grouped together into a symbol for a trellis code

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

4FSK	Four-level Frequency Shift Keying
AB	Appended Blocks
ACK	(positive) ACKnowledgement
AI	Air Interface
ARP	Address Resolution Protocol
ARQ	Automatic Retransmission reQuest
AT	Access Type
BCD	Binary Code Decimal
BER	Bit Error Rate
BF	Blocks to Follow
BOR	Beginning Of Receive
BPTC	Block Product Turbo Code
BS	Base Station

NOTE: A reference designating a fixed end device.

CACH	Common Announcement Channel
CC	Colour Code
CCL	Call Control Layer
C-plane	Control plane
CR	CRC bits
CRC	Cyclic Redundancy Checksum for data error detection
CS	CheckSum
CSBK	Control Signalling BlocK
CSBKO	CSBK Opcode
D_Sync	general Data burst Sync
DBSN	Data Block Serial Number
DD	Defined Data format
DLL	Data Link Layer
DMR	Digital Mobile Radio
DP	Destination Port
DPF	Data Packet Format
DT	Data Type field for General Data Bursts
EMB	EMBedded signalling field
Enc_Dibit	output Dibit from trellis Encoder
EOR	End Of Receive
ERC	European Radiocommunication Committee
ERM	Electromagnetic compatibility and Radio spectrum Matters
FEC	Forward Error Correction
FID	Feature set ID
FLCO	Full Link Control Opcode
FM	Frequency Modulation
FMF	Full Message Flag
FSM	Finite State Machine
FNS	Feature Not Supported

FSN	Fragment Sequence Number
GF	Galois Field to calculate parity checks for a RS code
GF(2)	Galois Field with 2 elements
Golay	Golay code parity check
H	Hamming parity bits
HC	Header Compression
H_Cx	Hamming parity bit from Column x of a BPTC
H_Rx	Hamming parity bit from Row x of a BPTC
HMSC	High level Message Sequence Chart
Hx	Hamming parity bit for row x of a BPTC
I	Information bit
ID	IDentifier
IP	Internet Protocol
ISO	International Standardization Organization
LB	Last Block
LBT	Listen Before Transmit
LC	Link Control
LCSS	Link Control Start/Stop
LLC	Logical Link Control
LLID	Logical Link ID
LSB	Least Significant Bit
LSO	Least Significant Octet
MAC	Medium Access Control
MBC	Multiple Block Control packets
MFID	Manufacturer's FID
MS	Mobile Station
MSB	Most Significant Bit
MSO	Most Significant Octet
NACK	Negative ACKnowledgement
NI	(sequence) Number Indicator
N_LC	Null LC bit
NMEA	National Maritime Electronic Association
N_xxxx	Layer 2 constant

NOTE: As defined in clause F.2.

OACSU	Off Air Call SetUp
P	CACH Payload
PA	Power Amplifier
PABX	Private Automatic Branch eXchange
PC	Parity Check bit
PDP	Packet Data Protocol
PDU	Protocol Data Unit
PF	Protect Flag
PI	Privacy Indicator

NOTE: When associated with PI Header OR Pre-emption and power control Indicator when an information element in EMB field.

PL	Physical Layer
ppm	parts per million
POC	Pad Octet Count
PR FILL	Pseudo-Random Fill bits
PSTN	Public Switched Telephone Network
QR	Quadratic Residue code parity check bit
R	Reserved bit
R_Sync	Reverse channel Sync
RC	Reverse Channel
RF	Radio Frequency
rms	root mean squared
RS	Reed-Solomon code
RSSI	Received Signal Strength Indication
RX	Receive

SAP	Service Access Point

NOTE: Where a network provides a service.

SAPID	SAP Identifier
SARQ	Selective Automatic Repeat reQuest
SB	Single Burst
SDL	Specification and Description Language
SF	Supplementary Flag
SFID	Standards FID
SLCO	Short Link Control Opcode
SMS	Short Message Service
SP	Source Port
SYNC	SYNChronization
T_xxxx	Layer 2 timer

NOTE: As defined in clause F.1.

TACT	TDMA Access Channel Type
TC	TDMA Channel
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
Trellis_Dibit	output Dibit from Trellis code
TX	Transmitted bit
UAB	UDT Appended Blocks
UTF	Unicode Transformation Format
UDP	User Datagram Protocol
UDT	Unified Data Transport
UDTO	UDT Opcode
U-plane	User plane
VF	Vocoder Frame
VI	(receiver) Variable Indicator
V_Sync	TDMA Voice burst Sync
VS	Vocoder Socket bit
WU	Wake Up

4 Overview

4.0 Overview introduction

The present document describes a Digital Mobile Radio (DMR) system for Tier I, Tier II and Tier III products which employs a Time Division Multiple Access (TDMA) technology with a 2-slot TDMA solution and RF carrier bandwidth of 12,5 kHz (see note 1).

NOTE 1: DMR system for Tier I products employs a continuous transmission variation of the above mentioned technology.

The present document describes the Physical Layer (PL) and the Data Link Layer (DLL) of the DMR Air Interface (AI). Radio equipments (fixed, mobile or portable) which conform to the present document shall be interoperable at the Air Interface with equipment from other manufacturers.

Slot formats, field definitions, and timing are defined for voice traffic, data traffic, and control signalling. An overview of the TDMA timing is provided followed by the basic slot formats and bit definitions. This is followed by definitions of the payload and control fields. Finally, the details of the modulation and timing constraints are specified.

The present document will not provide the specification or operational detail for system implementations which include but are not limited to trunking, roaming, network management, vocoder, security, data, subsystems interfaces and data between private and public switched telephone networks. It describes only the appropriate access requirements compatible with the Air Interface.

NOTE 2: The DMR standard consists of a multi-part deliverable, which will be referred to in the present document if needed.

4.1 Protocol architecture

4.1.0 Protocol architecture - Introduction

The purpose of this clause is to provide a model where the different functions and processes are identified and allocated to different layers in the DMR protocol stack.

The protocol stack in this clause and all other related clauses describe and specify the interfaces, but these stacks do not imply or restrict any implementation.

The DMR protocol architecture which is defined herein follows the generic layered structure, which is accepted for reference description and specification of layered communication architectures.

The DMR standard defines the protocols for the following 3 layered model as shown in figure 4.1.

The base of the protocol stack is the Physical Layer (PL) which is the layer 1.

The Data Link Layer (DLL), which is the layer 2, shall handle sharing of the medium by a number of users. At the DLL, the protocol stack shall be divided vertically into two parts, the User plane (U-plane), for transporting information without addressing capability (e.g. voice), and the Control plane (C-plane) for signalling information, both control and data, with addressing capability, as illustrated by figure 4.1.

NOTE 1: It is appropriate to bear in mind the different requirements of C-plane and U-plane information. C-plane information needs only a discrete (or non-continuous) physical link to pass information although it needs a continuous virtual link to support the service. This may also be called signalling or packet mode service. Acknowledgements may or may not be requested. U-plane information, on the other hand, requires a regular physical link to be available so that a constant delay service can be supported. This may also be called circuit mode service.

NOTE 2: The DLL identified in figure 4.1 may be further sub-divided in the air interface protocol to separate the functionality of Medium Access Control (MAC) and Logical Link Control (LLC), which is often performed in radio air interface protocols due to the specialized nature of these two tasks. Such separation is not presented in the present document and is implementation specific. It is further implementation specific if layer 2 at U-plane offers only MAC for the service.

The Call Control Layer (CCL), which is layer 3, lies in the C-plane and is responsible for control of the call (addressing, facilities, etc.), provides the services supported by DMR, and supports Short Data and Packet Data service. U-plane access at layer 2 (DLL) supports voice service which is available in DMR. The Control Layer and the facilities and services offered by DMR are described in ETSI TS 102 361-2 [5]. The Short Data and Packet Data Protocol offered by DMR are described in ETSI TS 102 361-3 [12].

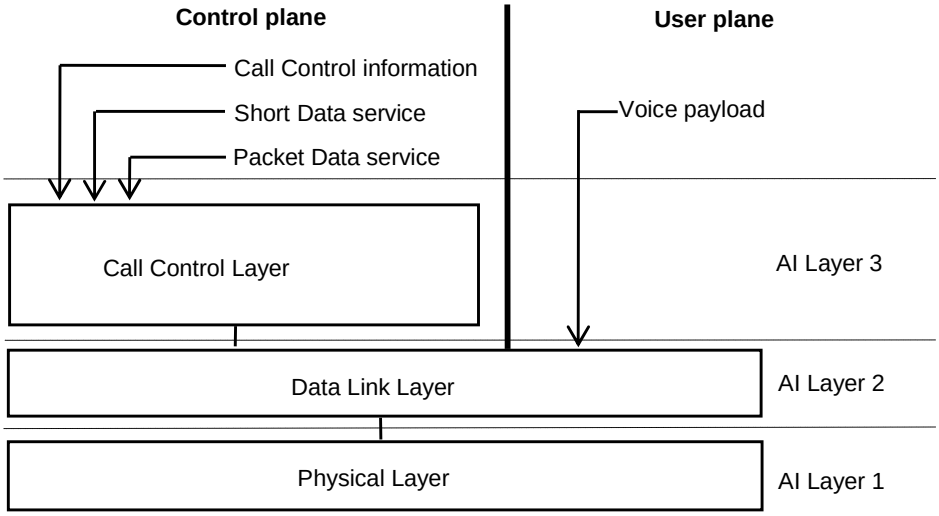


Figure 4.1: DMR protocol stack

4.1.1 Air Interface Physical Layer (layer 1)

The Air Interface layer 1 shall be the physical interface. It shall deal with the physical burst, composed of bits, which is to be sent and/or received. The Physical Layer is described in clause 10.

The Air Interface layer 1 shall contain the following functions:

- modulation and demodulation;
- transmitter and receiver switching;
- RF characteristics;
- bits and symbol definition;
- frequency and symbol synchronization;
- burst building.

4.1.2 Air Interface Data Link Layer (layer 2)

The Air Interface layer 2 shall handle logical connections and shall hide the physical medium from the upper layers. The Data Link Layer is described in clauses 5 to 9.

The main functions are as follows:

- channel coding (FEC, CRC);
- interleaving, de-interleaving and bit ordering;
- acknowledgement and retry mechanism;
- media access control and channel management;
- framing, superframe building and synchronization;
- burst and parameter definition;
- link addressing (source and/or destination);
- interfacing of voice applications (vocoder data) with the PL;
- data bearer services;
- exchanging signalling and/or user data with the CCL.

4.1.3 Air Interface Call Control Layer (CCL) (layer 3)

Air Interface layer 3 (CCL) is applicable only to the C-plane, and shall be an entity for the services and facilities supported by DMR on top of the layer 2 functionality. The Call Control Layer (CCL) is described in ETSI TS 102 361-2 [5] and may have embedded intrinsic services associated to it.

The CCL provides the following functions:

- BS activation / deactivation;
- establishing, maintaining and terminating of calls;
- individual or group call transmission and reception;
- destination addressing (DMR IDs or gateway as appropriate);
- support of intrinsic services (emergency signalling, pre-emption, late entry, etc.);
- data call control;
- announcement signalling.

4.2 DMR TDMA structure

4.2.1 Overview of burst and channel structure

The described solution is based on a 2-slot TDMA structure.

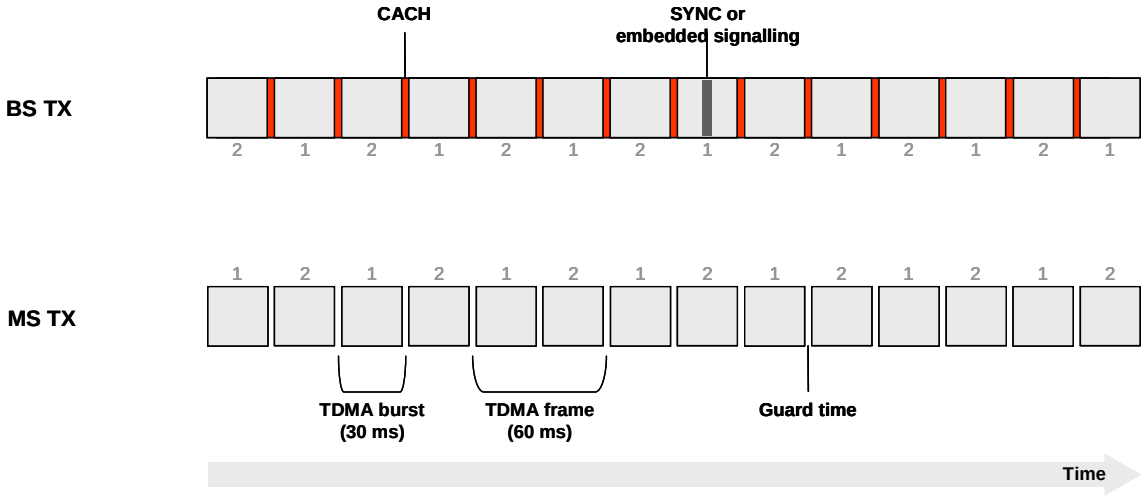
The physical resource available to the radio system is an allocation of the radio spectrum. The radio spectrum allocation shall be partitioned into Radio Frequency (RF) carriers with each RF carrier partitioned in time into frames and timeslots.

A DMR burst is a period of RF carrier that is modulated by a data stream. A burst therefore represents the physical channel of a timeslot. The physical channel of a DMR subsystem is required to support the logical channels.

A logical channel is defined as a logical communication pathway between two or more parties. The logical channels represent the interface between the protocol and the radio subsystem. The logical channels may be separated into two categories:

- the traffic channels carrying speech or data information; and
- control channels carrying signalling.

A generalized timing diagram of exchanges between the MS and the BS is shown in figure 4.2 where the slots for the two TDMA physical channels are labelled channel "1" and "2". Inbound transmission is labelled "MS TX" and outbound transmission is labelled "BS TX". Figure 4.2 is intended to illustrate a number of signalling features and timing relationships and does not represent a particular scenario.



NOTE: The example timing in figure 4.2 applies to a two frequency BS.

Figure 4.2: TDMA timing overview

Key points illustrated by the figure 4.2 include:

- While the BS is actively transmitting, the outbound channel is continuously transmitted, even if there is no information to send. Transmission on the inbound channel is stopped when an MS has no information to transmit.
- The inbound channel has an unused guard time between bursts to allow Power Amplifier (PA) ramping and propagation delay.
- The outbound channel has a Common Announcement Channel (CACH) between bursts for traffic channel management (framing and access) as well as low speed signalling.
- Bursts have either a synchronization pattern or an embedded signalling field located in the centre of the burst. Placing the embedded signalling in the middle of a burst allows time for a transmitting MS to optionally transition to the outbound channel and recover Reverse Channel (RC) information.

Other key points, summarized below but not limited to, are as follows:

- The centre of the inbound and outbound bursts shall be time aligned.
- The channel 1 and 2 bursts in the inbound channel are offset 30 ms in time from the channel 1 and 2 bursts in the outbound channel. This number scheme allows a single channel identifier field in the outbound CACH to use the same channel number when referring to the inbound and outbound channels.
- Different SYNC patterns are used in voice bursts and data bursts to allow the receiver to differentiate between them. Different SYNC patterns are used for inbound and outbound channels to help the receiver reject co-channel interference.

- A Colour Code (CC) is present in the embedded signalling field and general data burst to provide a simple means of distinguishing overlapping sites, in order to detect co-channel interference.

NOTE: The CC is not used for addressing (individual or group).

- The location of the SYNC bursts in channel 1 is independent from the location of the SYNC bursts in channel 2. The location of SYNC bursts in the inbound channels is independent from the location of the SYNC bursts in the outbound channels.
- Voice transmissions use a superframe that is 6 bursts (360 ms) long with bursts labelled "A" to "F". Each superframe starts with a voice synchronization pattern in burst A.
- Data and control do not have a superframe structure. These bursts may contain a synchronization pattern and may also carry embedded signalling, such as RC, when required.

4.2.2 Burst and frame structure

The generic burst structure consists of two 108-bit payload fields and a 48-bit synchronization or signalling field as shown in figure 4.3. Each burst has a total length of 30 ms but 27,5 ms are used for the 264 bits content, which is sufficient to carry 60 ms of compressed speech, using 216 bits payload.

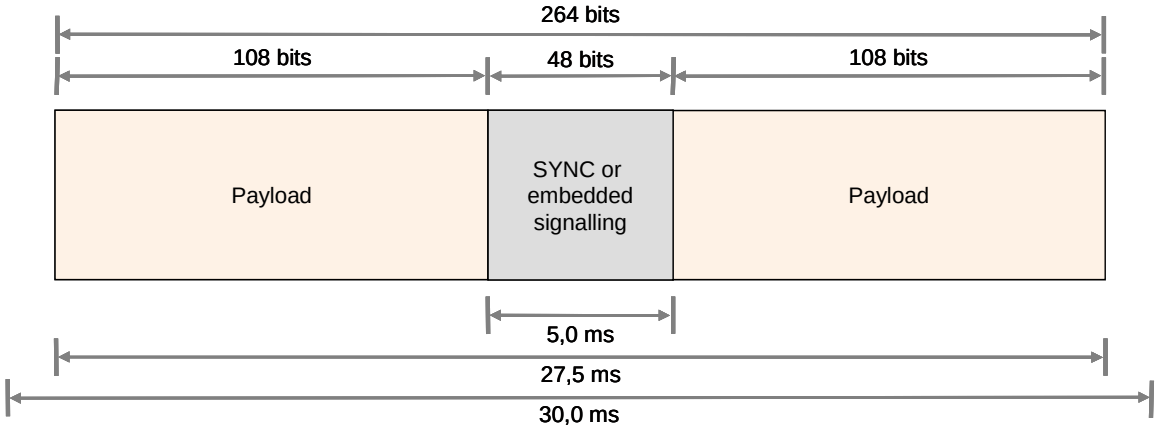


Figure 4.3: Generic burst structure

For example, for a vocoder that uses 20 ms vocoder frames, the burst will carry three 72-bit vocoder frames (including FEC) plus a 48-bit synchronization word in a voice burst, that is 264 bits (27,5 ms) used for the burst contents.

NOTE: For data and control information the payload is reduced to two 98-bit payload which left a 20-bit field for additional Data Type field definition, as described in clause 6.2.

The centre of each burst has a field that carries either synchronization or embedded signalling. This field is placed in the middle of a burst to support RC signalling (see clause 5.1.5).

On the inbound channel, the remaining 2,5 ms is used for guard time to allow for PA ramping and propagation delay, as shown in figure 4.4 for an inbound frame.

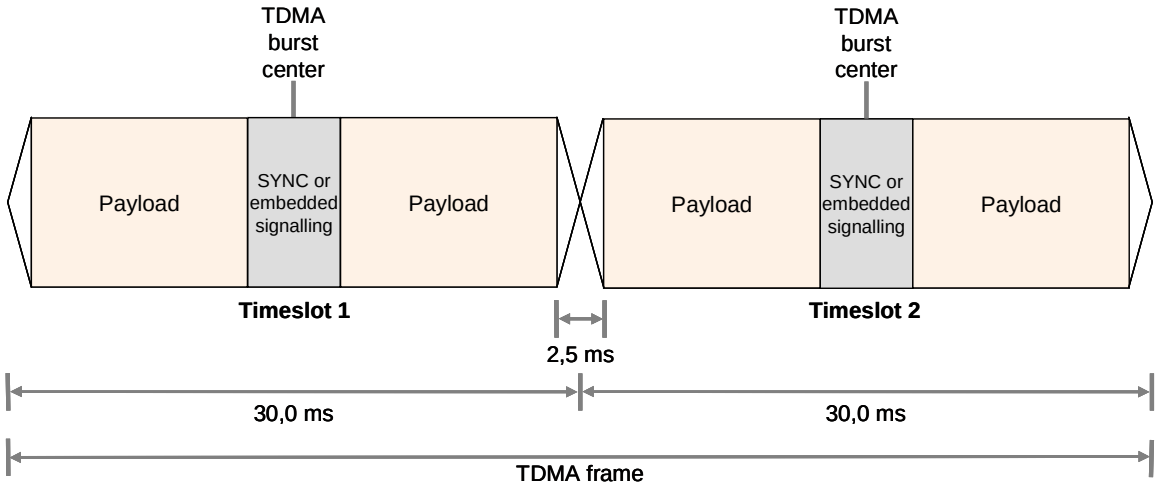


Figure 4.4: MS sourced TDMA frame

On the outbound channel, this 2,5 ms is used for a Common Announcement Channel (CACH) that carries TDMA frame numbering, channel access indicators, and low speed signalling as shown in figure 4.5 for an outbound frame.

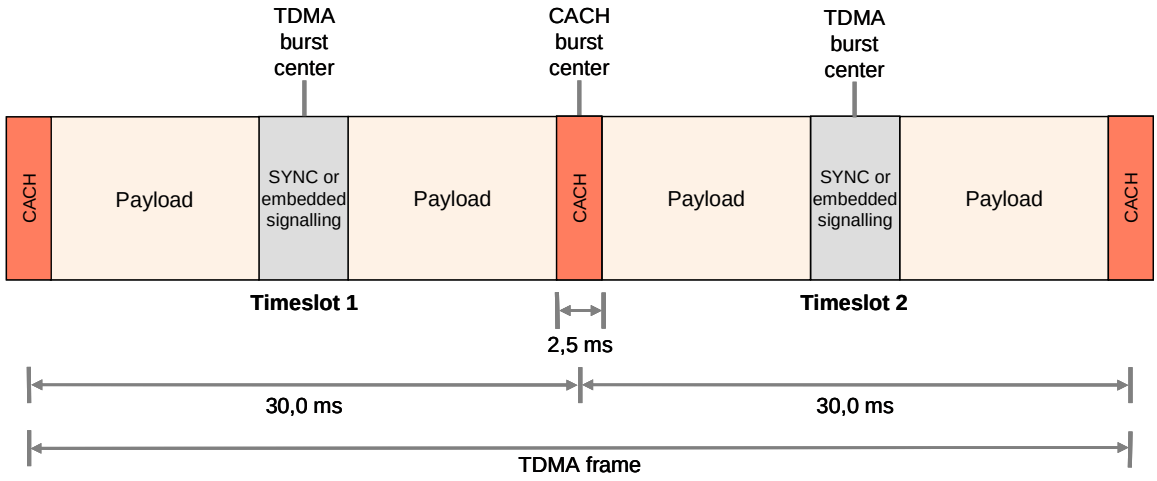


Figure 4.5: BS sourced TDMA frame

4.3 Frame synchronization

Frame SYNChronization (SYNC) is provided by a special sequence of bits that mark the location of the centre of a TDMA burst. Receivers may use a matched filter to achieve initial synchronization, using the output of a matched correlator to initialize the symbol recovery parameters to compensate for frequency and deviation errors as well as determine the centre of the burst. Once the receiver is synchronized to a channel, it may use pattern matching to detect the presence of SYNC to verify that the channel is still present and determine the type of SYNC to identify the contents of the burst. Multiple SYNC patterns are used to:

- differentiate voice bursts from data/control bursts and from RC bursts;
- differentiate inbound channels from outbound channels;
- differentiate repeater channels from TDMA direct mode time slots;
- differentiate TDMA direct mode time slot 1 from TDMA direct mode time slot 2.

To accomplish this, the following SYNC patterns have been defined (see clause 9.1.1 for details and bit patterns for the frame SYNC):

- BS sourced voice;
- BS sourced data;
- MS sourced voice;
- MS sourced data;
- MS sourced standalone RC.
- TDMA direct mode time slot 1 voice;
- TDMA direct mode time slot 1 data;
- TDMA direct mode time slot 2 voice;
- TDMA direct mode time slot 2 data.

For all two frequency BS channel inbound transmissions and all single frequency channel transmissions, the first burst shall contain a synchronization pattern to allow the target receiver to detect the presence of the signal, achieve bit synchronization, and determine the centre of the burst. Follow-on bursts contain either SYNC or embedded signalling depending on the burst type and the context.

For data and control messages, the embedded field shall be only a data SYNC pattern or RC signalling (see clauses 5.1.5.1 and 5.1.5.2). For voice calls, the voice SYNC pattern occurs in the first burst of every voice superframe. In addition to marking the superframe boundaries, periodically inserting these periodic syncs allow late entry receivers to pick up voice messages after the transmission has started. See clause 5.1.2.1 for details on the superframe structure.

Figure 4.6 illustrates the best case and worst-case synchronization period for an inbound (MS to BS) TDMA channel. Since data and control messages contain a frame synchronization field in each burst, SYNC opportunities can occur as frequently as every 60 ms. During a voice call, SYNC opportunities occur every 360 ms, the length of a voice superframe. The first burst of every inbound transmission shall contain a SYNC pattern in order to allow the target to detect and synchronize to the transmission.

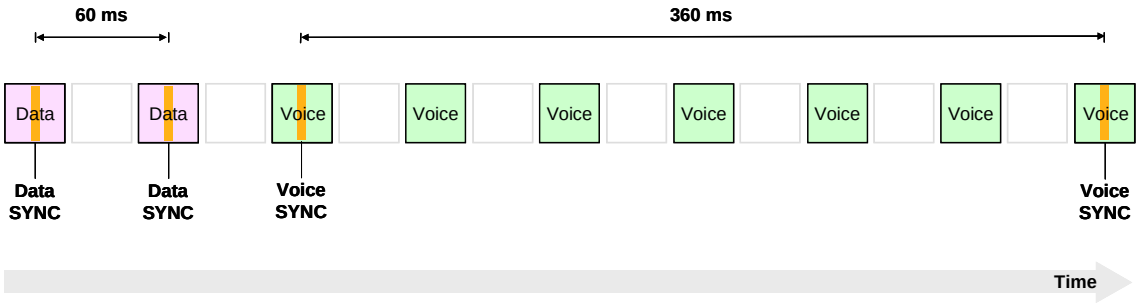


Figure 4.6: Inbound synchronization timing

Figure 4.7 illustrates the best case and worst-case synchronization period for an outbound (BS to MS) TDMA channel. Because an outbound channel is continuously keyed, both TDMA channels always contain some type of signalling. In addition, since the target MS can receive both TDMA slots, the target MS can detect SYNC in either slot. Because data and control messages will typically contain a frame synchronization field in each burst, SYNC opportunities can occur as frequently as every 30 ms. During a voice call, SYNC opportunities occur every 360 ms, the length of a voice superframe, on each channel.

Figure 4.7 illustrates the worst-case SYNC timing for voice, 330 ms, which occurs when two voice calls are active and their superframes (for details of superframes see clause 5.1.2.1) are offset by 30 ms.

Based on these assumptions, the time between SYNC opportunities can be as short as 30 ms and as long as 330 ms.

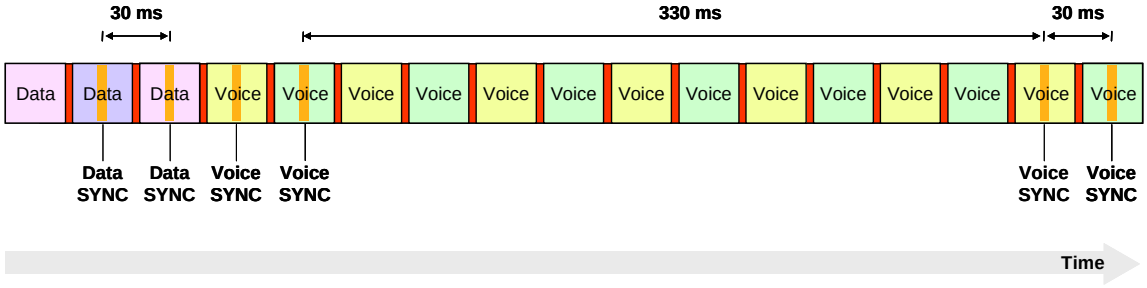


Figure 4.7: Outbound synchronization timing

4.4 Timing references

4.4.1 Repeater mode BS established timing relationship

When operating with a BS, a MS shall synchronize to an outbound channel and base its inbound timing entirely on the outbound timing. This insures that all MS units are working off of the same timing reference. If the BS is not currently transmitting, a MS wishing to access the system shall send a "BS activation" signalling to the BS asynchronously and wait for the outbound channel to be established before synchronizing and continuing with further transmission (see ETSI TS 102 361-2 [5]).

4.4.2 Repeater mode MS established timing relationship

When operating with a BS, it is also possible to have BSs that are able to transmit their outbound channel in a way that is synchronized with an MS inbound channel avoiding the "BS activation" procedure. Also this BS behaviour insures that all MS units are working off of the same timing reference.

4.4.3 Direct mode timing relationship

In direct mode, the transmitting MS shall establish the timing reference. Any MS wishing to send RC signalling back to the source shall synchronize to the forward path and shall base their RC timing on the forward path timing. Once the source MS stops transmitting, any other MS wishing to transmit shall begin sending information asynchronously and establish a new and independent time reference.

NOTE: RC signalling applies only for Tier II and Tier III products.

4.4.4 TDMA direct mode timing relationship

In TDMA direct mode, an elected channel timing leader MS shall establish the timing reference for both time slots on the frequency. MS units that are not the channel timing leader are responsible for retransmitting the timing reference out to the edge of the wide area system. This mechanism helps to ensure that all MS units in the wide area system are working from the same timing reference. In general a MS transmits in the appropriate slot with the channel slot timing established by the channel timing leader MS.

4.5 Common Announcement Channel (CACH)

While the inbound channel requires an unused guard time between bursts to allow PA ramping and propagation delay, the outbound channel from the BS shall transmit continuously after BS activation and utilize this small segment for additional signalling. A Common Announcement Channel (CACH) is defined between the outbound bursts and is used for channel management (framing and access) as well as for low speed signalling.

One purpose of the CACH is to indicate the usage of the inbound time slot. Since a two frequency BS is full-duplex it transmits simultaneously while it is receiving and shall send status information to all of the listening MS units about the channel status (idle or busy) of the inbound time slot. When a MS unit wishes to transmit a data message, it shall wait until the inbound time slot is flagged as Channel State Idle (CS_Idle) before it transmits.

Figure 4.8 shows the timing relationship between a particular CACH burst and its corresponding inbound time slot. Each CACH burst indicates the status of the inbound time slot delayed by one slot to allow the receiver time to receive the CACH, decode the information, decide what action to take, and transition to transmit mode. In the example shown, the CACH burst preceding outbound time slot 2 bursts indicates the status of the burst in inbound time slot 2.

NOTE: This timing relationship is based on the shortest time period that can be used in practice.

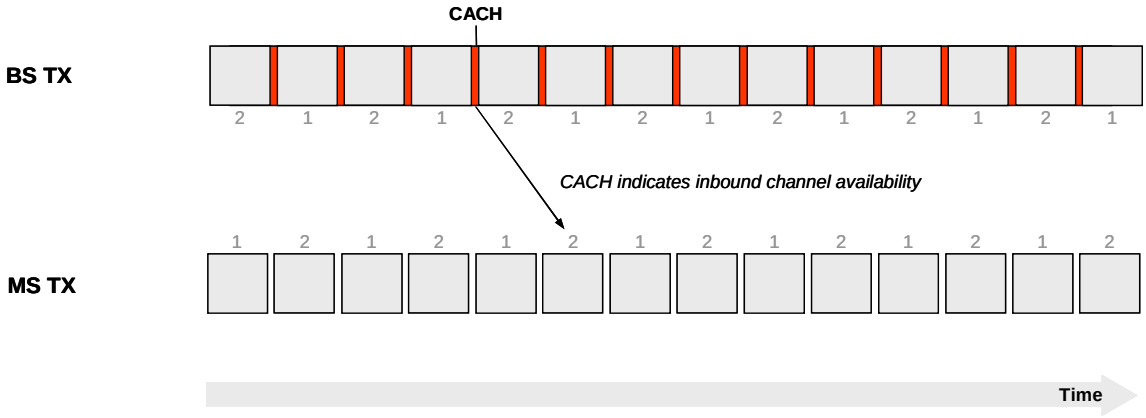


Figure 4.8: Access type indicator timing

A second purpose of the CACH is to indicate the channel number of the inbound and outbound time slots as illustrated in figure 4.9. Each CACH burst defines the channel number for the outbound time slot immediately following and the inbound time slot delayed by one slot. In the example shown, the CACH burst indicates the position of inbound time slot 2 and outbound time slot 2.

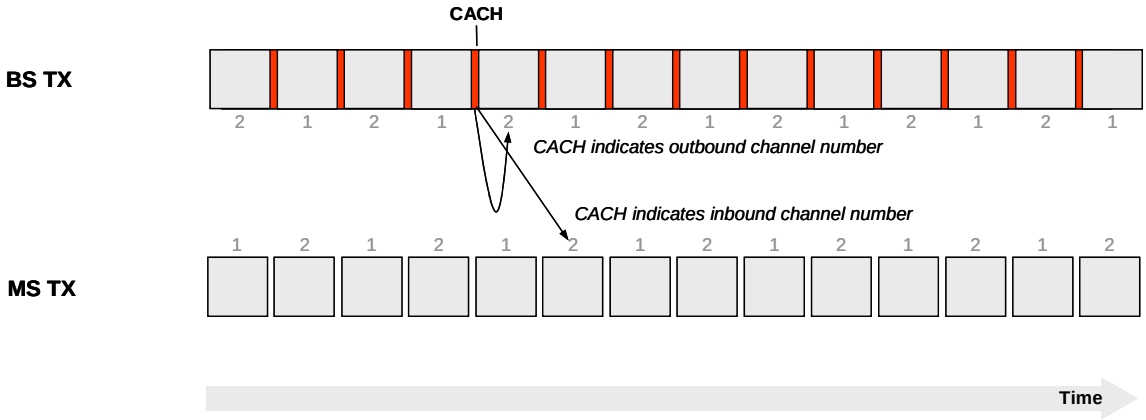


Figure 4.9: CACH channel indicator timing

A third purpose of the CACH is to carry additional low speed signalling as described in clause 7.1.4.

4.6 Basic channel types

4.6.1 Traffic channel with CACH

The traffic channel with CACH is shown in figure 4.10. This channel type shall be used for outbound transmissions from a two frequency BS to a MS. The physical channel consists of two TDMA outbound channels (time slots 1 and 2) as well as a CACH for channel numbering, channel access, and low speed data. This physical channel is transmitted continuously without gaps as long as the BS is activated.

If no information is available to transmit in outbound time slot 1 and/or outbound time slot 2, the BS shall transmit Idle messages to fill out the bursts (see clause 7.3).

If no CACH payload is available to transmit, Null message Short LCs shall be sent as defined in ETSI TS 102 361-2 [5]. For the transmission of Null message Short LC in CACH see clause 7.1.4.

NOTE: This channel type should also be used for continuous transmission mode between MS units.

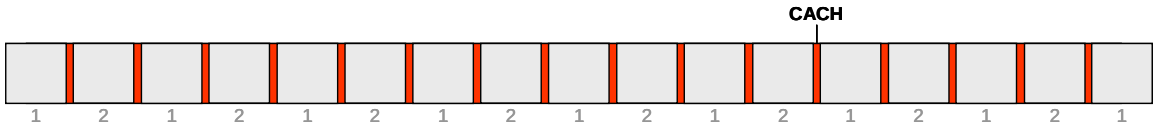


Figure 4.10: Traffic channel with CACH

4.6.2 Traffic channel with guard time

The traffic channel with guard time is shown in figure 4.11. This channel type shall be used for inbound transmissions from a MS to a two frequency BS (see note) and for TDMA direct mode transmissions. The channel consists of two TDMA traffic channels (time slots 1 and 2) separated by a guard time to allow PA ramping and propagation delay. Three use cases are shown for this channel type:

Use Case 1: Both time slots utilized for traffic (see note).

Use Case 2: A single time slot (slot 1) utilized for traffic.

Use Case 3: One time slot utilized for traffic (time slot 2) while the other is used for short standalone RC bursts (time slot 1).

NOTE: The first use case should also be used for communication via a single frequency BS where time slot is MS to BS and time slot 2 is BS to MS, or vice versa.

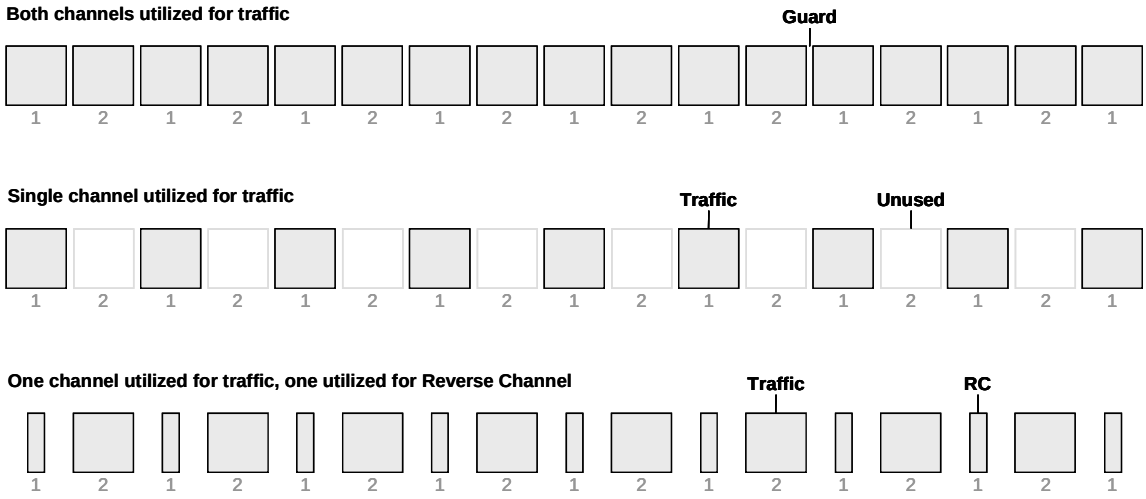


Figure 4.11: Traffic channel with guard time

4.6.3 Bi-directional channel

The bi-directional channel is shown in figure 4.12. This channel type is used for direct mode communication between MS units. The channel consists of a Forward and a Backward TDMA traffic channels on the same frequency separated by guard times. Three use cases are shown for this channel type:

Use Case 1: Both time slots utilized for duplex traffic (Forward and Backward).

Use Case 2: A single time slot (Forward) utilized for traffic.

Use Case 3: One time slot utilized for traffic (Forward) while the other time slot is used for short RC signalling (Reverse).

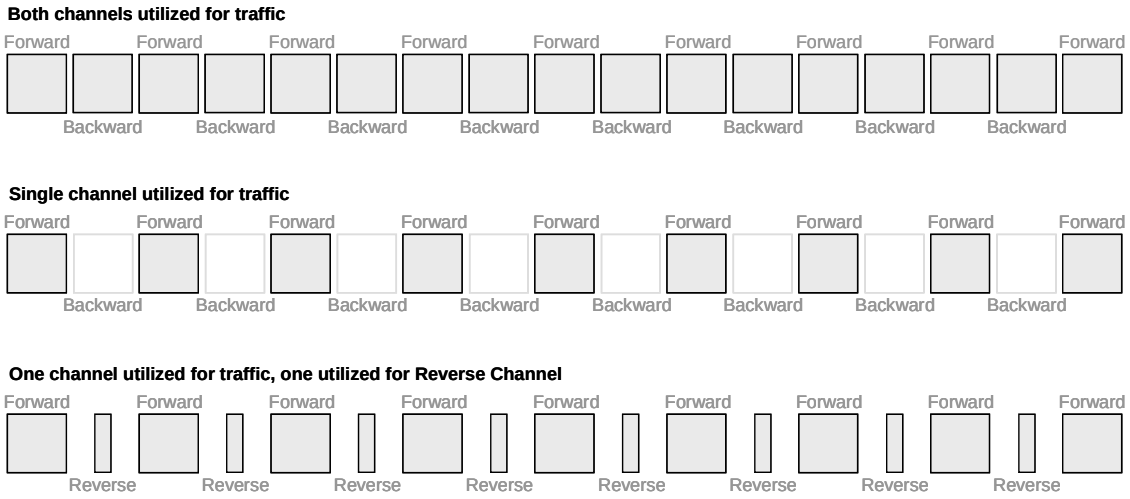


Figure 4.12: Bi-directional channel

5 Layer 2 protocol description

5.0 Layer 2 protocol description - Introduction

The following clauses describe the layer 2 protocol and define the operation of the Data Link Layer (DLL) of the DMR Air Interface (AI). The protocol description is made in terms of the timing relationship and the channel access rules.

5.1 Layer 2 timing

5.1.1 Channel timing relationship

5.1.1.0 Channel timing relationship - Introduction

The channel designation of "1" and "2" refer to logical channels that have a strictly defined relationship. The inbound channel 1 and 2 time slots are offset in time from the outbound channel 1 and 2 time slots. Various call types and services can require specific timing relationships between the inbound and outbound channels which lead to the definition of a number of logical channels.

Voice and data sessions require both an inbound time slot and an outbound time slot. The timing relationship between the inbound time slot and the outbound time slot can be either aligned in time (aligned channels) or non-aligned (offset channels) as described in clauses 5.1.1.1 and 5.1.1.2 of the present document. MSs shall be aware if aligned channel timing or offset channel timing is expected by the BS. The logical channel relationship to the inbound and outbound time slots for both aligned channel timing and offset channel timing shall conform to table 5.1.

Table 5.1: Logical channel relationship to inbound and outbound channels

Channel Timing	Logical Channel	Inbound Time Slot (MS TX)	Outbound Time Slot (BS TX)
Aligned	1	2	1
	2	1	2
Offset	1	1	1
	2	2	2

5.1.1.1 Aligned channel timing

Aligned timing supports RC signalling by providing the receiving MS with a RC transmit opportunity on the inbound time slot without missing any of its outbound traffic. The example in figure 5.1 illustrates transmissions on logical channel 1, which consists of inbound time slot 2 and outbound time slot 1. Therefore an MS provisioned to only receive and transmit on logical channel 1 shall receive on outbound time slot 1 and shall transmit on inbound time slot 2 when the BS channel timing is aligned. Likewise, an MS provisioned to only receive and transmit on logical channel 2 shall receive on outbound time slot 2 and shall transmit on inbound time slot 1 when the BS channel timing is aligned.

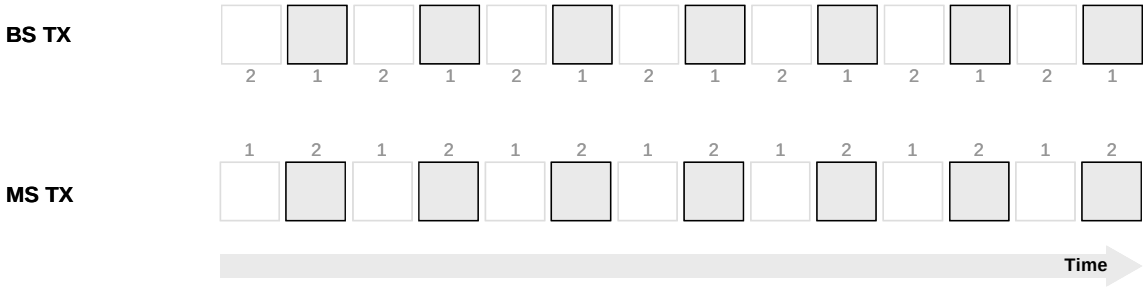


Figure 5.1: Aligned channel timing

NOTE: MS to MS timing requirements apply when communicating through a BS.

5.1.1.2 Offset channel timing

Offset timing supports duplex traffic by allowing a MS to transmit inbound on one time slot and receive the outbound transmission on the alternate time slot (see clause 5.1.4.4). The example in figure 5.2 illustrates transmissions on logical channel 1, which consists of inbound time slot 1 and outbound time slot 1. Therefore an MS provisioned to only receive and transmit on logical channel 1 shall receive on outbound ctime slot 1 and shall transmit on inbound time slot 1 when the BS channel timing is offset. Likewise, an MS provisioned to only receive and transmit on logical channel 2 shall receive on outbound time slot 2 and shall transmit on inbound time slot 2 when the BS channel timing is offset.

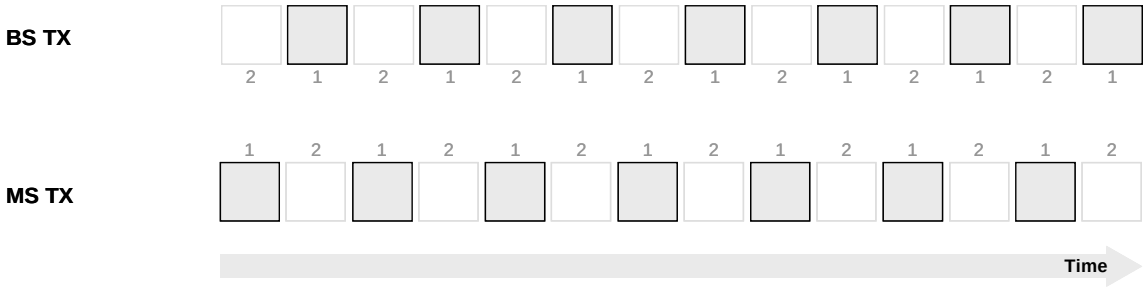


Figure 5.2: Offset channel timing

5.1.2 Voice timing

5.1.2.1 Voice superframe

Vocoder frames shall be transmitted using a six burst, 360 ms, superframe as shown in figure 5.3. Complete TDMA superframes are repeated for the duration of the voice message. The bursts of a superframe are designated with letters "A" through "F". Burst A marks the start of a superframe and always contains a voice SYNC pattern. Bursts B to F carry embedded signalling in place of the SYNC pattern.

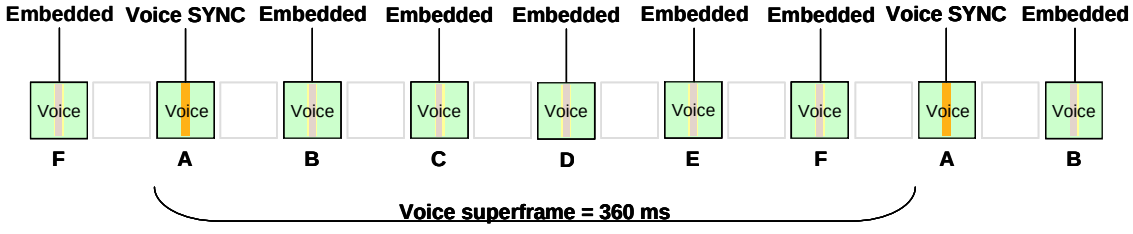


Figure 5.3: Voice superframe

5.1.2.2 Voice initiation

For conventional systems the first burst A of a voice transmissions and a repeated voice transmission shall only be immediately preceded by a voice LC header or a PI header. The sequence of information during voice initiation with only a voice LC header is shown in figure 5.4. The voice message begins with a voice LC header burst, and then continues with voice superframes. Details of the LC header are given in clause 7.1.

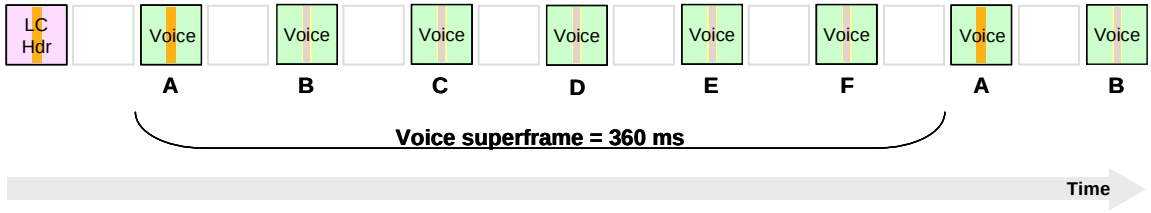


Figure 5.4: Voice initiation with LC header

In trunked systems voice may be transmitted without any preceding header as shown in figure 5.5. Other MS units on the traffic channel can determine the source and destination groups/units based on trunking control signalling.

NOTE 1: Not having to transmit the preceding header allows the initial speech delay to be reduced. However, MSs and BSs will only be permitted to omit the preceding header if this feature is supported by the system configuration.

NOTE 2: Using a preceding LC header in trunked systems is optional.

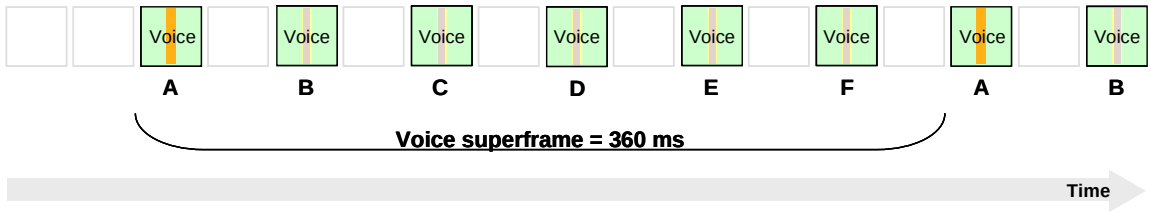


Figure 5.5: Voice initiation without header

For conventional systems a voice LC header shall be sent and a PI header may be sent at the beginning of the voice transmission as illustrated in figure 5.6. In this case, the voice LC header shall precede the PI header.

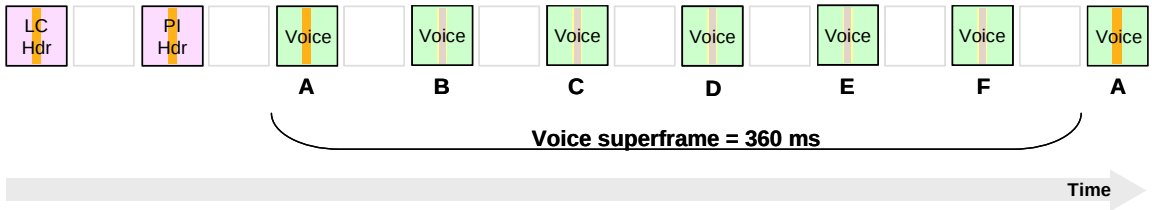


Figure 5.6: Voice initiation with LC and PI header

For trunked systems a PI header may be sent at the beginning of the voice transmission to indicate privacy status and properly initialize any privacy functions. The sequence of information is shown in figure 5.7. To support late entry, additional privacy information may be interleaved throughout the voice message.

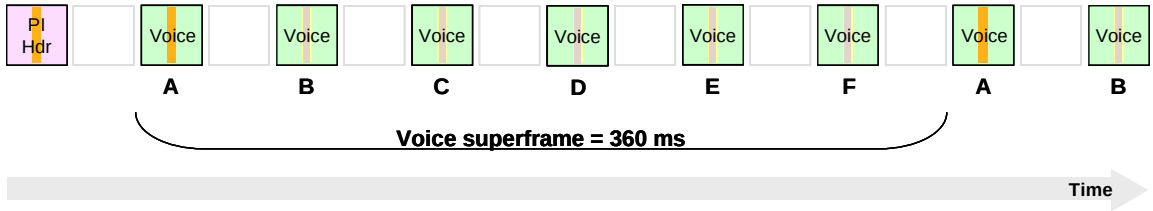


Figure 5.7: Voice initiation with PI header

5.1.2.3 Voice termination

Voice transmission speech items shall be terminated by sending a general data burst with a data SYNC pattern instead of a voice SYNC pattern in the burst immediately following the end of a voice superframe. This is illustrated in figure 5.8.

NOTE 1: For an inbound (two or single frequency) BS channel and direct mode a terminator with LC is used for the general data burst. In all other cases, the voice termination with LC may be used in the general data burst.

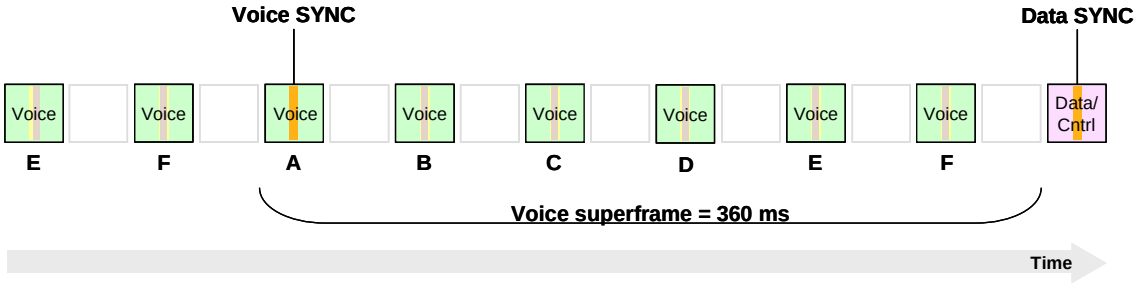


Figure 5.8: Voice termination

Since the data SYNC is sufficient to indicate the end of a voice transmission speech item, any general data burst shall work as a terminator message.

NOTE 2: It is up to the implementation whether to process the data burst or use the SYNC as terminator.

5.1.3 Data timing

5.1.3.0 Data timing - Introduction

The present document defines single slot and dual slot data transmission modes. The differences between these two modes are only the bit rate offered to upper layers of the DMR stack leaving unchanged the format of the carried messages.

NOTE: It is a function of system implementation which data transmission modes are used.

5.1.3.1 Single slot data timing

Figure 5.9 illustrates one example of timing for single slot inbound data transmission. The single slot data transmission shall be initiated with one or two data headers that contain addressing as well as information about the payload. These headers are followed by one or more data blocks. The last block in the transmission terminates the entire data message transfer. A complete description of the data transmission possibilities will be presented in ETSI TS 102 361-3 [12].

Figure 5.9 illustrates an exchange between a MS and the infrastructure where a single data header is required.

Figure 5.9: Single header data timing

Figure 5.10 illustrates a single slot inbound data transmission exchange between two MS for which two data headers are required.

Figure 5.10: Dual header data timing

The single slot data transmission mode is applicable to:

- direct channels; or
- single frequency repeater; or

- 1:1 repeater systems with RC; or
- 1:1 repeater systems with no RC; or
- 2:1 repeater systems.

5.1.3.2 Dual slot data timing

Figure 5.11 illustrates the timing for an outbound dual slot data occurrences. This example illustrates a transmission initiated with one data header. The header is followed by one or more data blocks (twelve in this example). The last block in the transmission contains payload and CRC to verify that the entire data message was successfully transferred.

NOTE: A complete description of the data transmission possibilities will be presented in ETSI TS 102 361-3 [12].

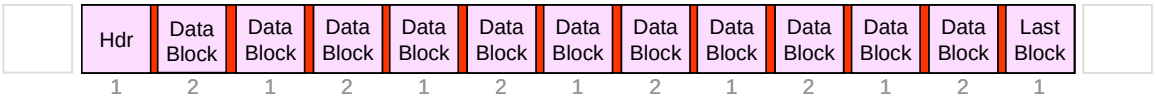


Figure 5.11: Dual slot data timing

The dual slot data transmission mode is applicable to:

- direct channels; or
- 1:1 repeater systems with no RC.

5.1.4 Traffic timing

5.1.4.1 BS timing

The following figures illustrate example timings for repeated traffic. The repeat delay will be based on the type of logical channel used (offset or aligned channels) as well as the ability of the BS to process the information.

NOTE: Some BS or system implementations can result in longer timing delays than those shown in the following examples.

Figure 5.12 shows an example timing diagram for repeated traffic using aligned traffic channels. In this example, the MS transmits on inbound channel 2 and receive on outbound channel 1. Consequently, there is an inherent 60 ms delay in the repeat path.

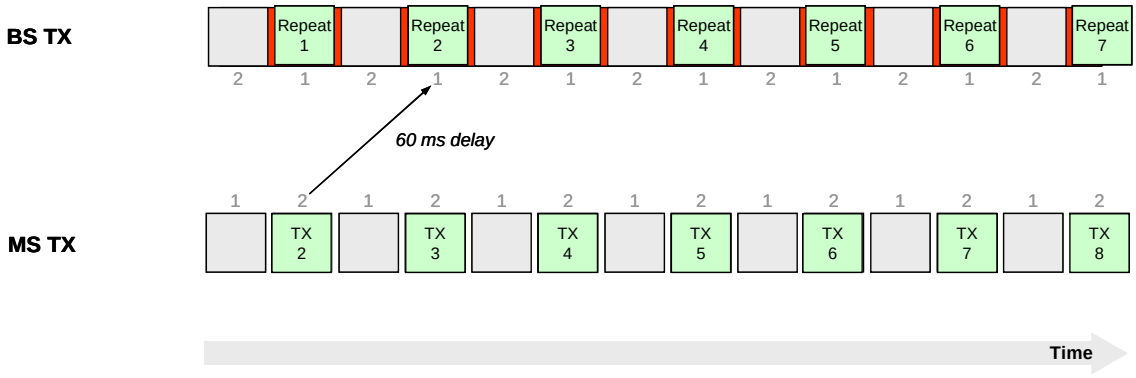


Figure 5.12: Aligned channels BS timing

Figures 5.13 and 5.14 show example timing diagrams for repeated traffic using Offset traffic channels. In these examples, the MS transmit on the inbound channel 2 and listen to the outbound channel 2. If the BS is capable of processing the inbound traffic and repeating it on the next outbound slot, there will be a 30 ms delay in the repeat path as shown in figure 5.13.

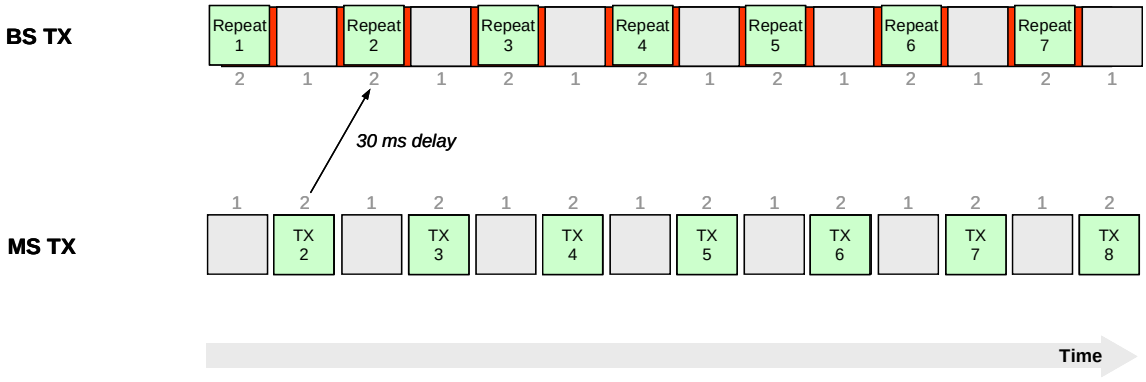


Figure 5.13: Offset channels repeated voice timing - 30 ms delay

If the BS is not capable of processing the inbound traffic and repeating it on the next outbound slot, there will be at least a 90 ms delay in the repeat path as shown in figure 5.14.

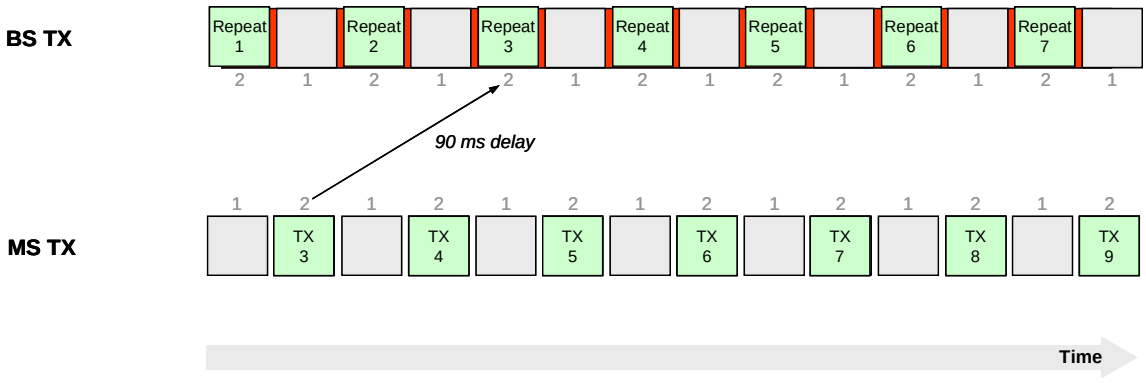


Figure 5.14: Offset channels repeated voice timing - 90 ms delay

5.1.4.2 Single frequency BS timing

Figure 5.15 illustrates an example timing diagram for a single frequency BS. In this example, the MS transmits on the inbound channel, which is one of the TDMA physical channels. The BS re-transmits the outbound voice on the alternate TDMA channel.

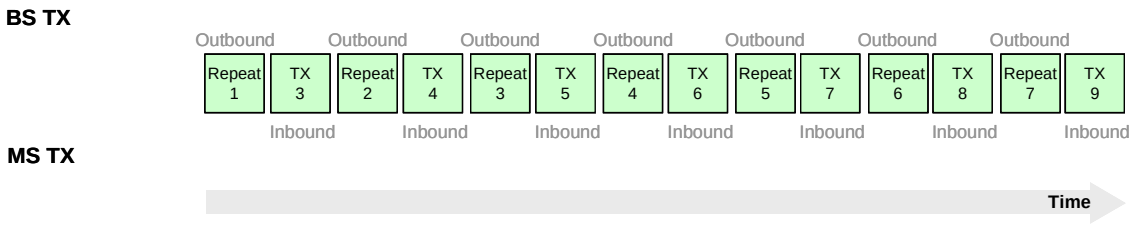


Figure 5.15: Single frequency BS timing

If the BS is not capable of processing the inbound traffic and repeating it on the next outbound slot, there will be a 3 burst (90 ms) delay in the repeat path as shown.

5.1.4.3 Direct mode timing

Figure 5.16 illustrates an example timing diagram for direct mode traffic. In this example, the MS transmits on the forward channel, which is one of the TDMA physical channels.

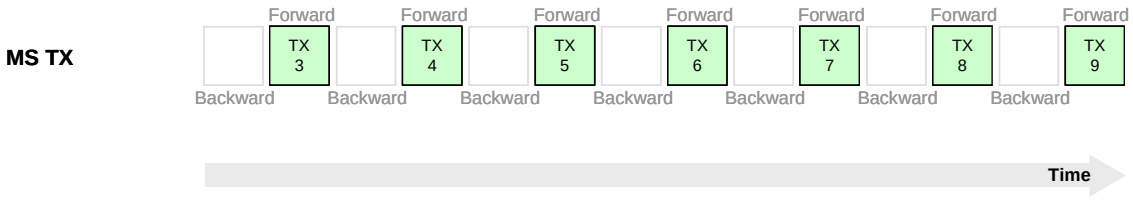


Figure 5.16: Direct mode timing

5.1.4.4 Time Division Duplex (TDD) timing

Figure 5.17 shows an example timing diagram for TDD (duplex) voice. In this example, the MS transmits voice on inbound channel 2 and listen to voice on the outbound channel 2.

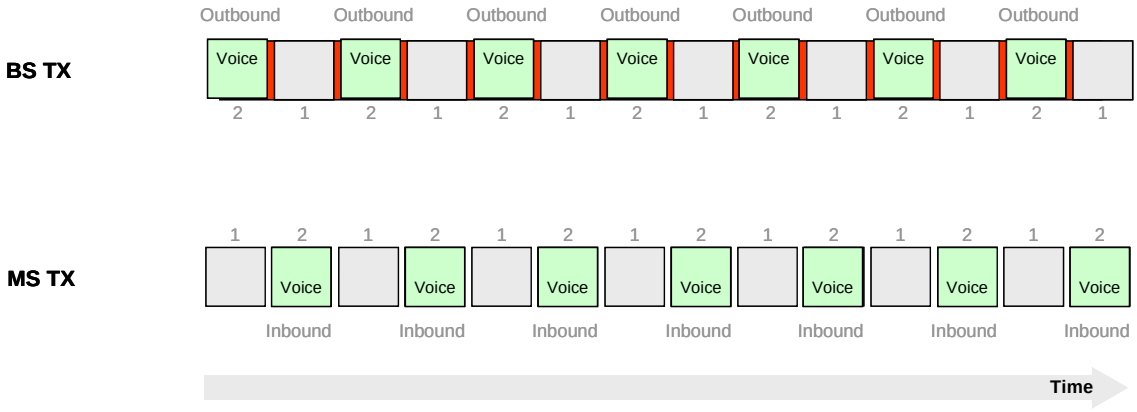


Figure 5.17: TDD voice timing

5.1.4.5 Continuous transmission mode

The format for Continuous Transmission uses the "Traffic Channel with CACH" defined in clause 4.6.1. In this mode, however, two traffic channels and the CACH are transmitted by a MS instead of a BS. In order to completely fill the channel, identical traffic is sent on both channel 1 and channel 2. Link Control signalling can be sent via the CACH if desired. Since there is no BS, only MS sourced SYNC patterns are used.

An example of continuous transmission for voice is illustrated in figure 5.18. This example shows a call initiated on channel 1 using an LC header, lasting a single voice superframe, and ending with a Terminator with LC. Voice traffic is sent using the inbound voice superframe defined in clause 5.1.2.1. Identical traffic is sent one burst later in channel 2 as shown.

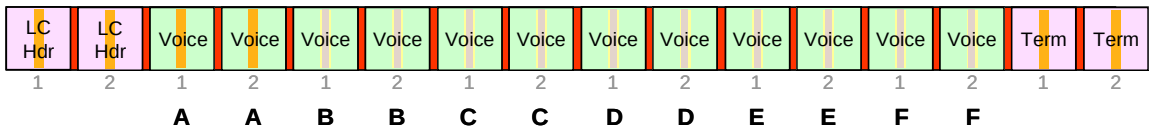


Figure 5.18: Continuous transmission mode for voice

An example of continuous transmission for data is illustrated in figure 5.19. This example shows a data transaction on channel 1 initiated, lasting five data blocks, and ending with a Last Data Block. Identical traffic is sent one burst later in channel 2 as shown.

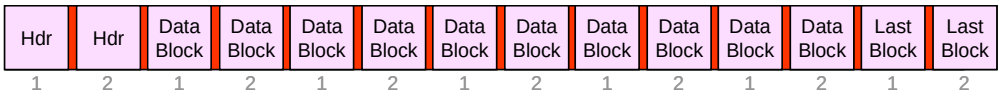


Figure 5.19: Continuous transmission mode for data

If no CACH payload is available to transmit, Null message Short LCs shall be send as defined in ETSI TS 102 361-2 [5]. For the transmission of Null message Short LC in CACH, see clause 7.1.4.

When the MS transmits in continuous transmission mode it shall set the CACH AT information element to busy and the CACH TC information element to alternate between 0_2 and 1_2.

NOTE: Continuous transmission mode is applicable only to Tier I products.

5.1.4.6 TDMA direct mode timing

Figure 5.20 illustrates an example timing diagram for TDMA direct mode traffic. In this example, the MS transmits on time slot 2, which is one of the two TDMA logical channels.

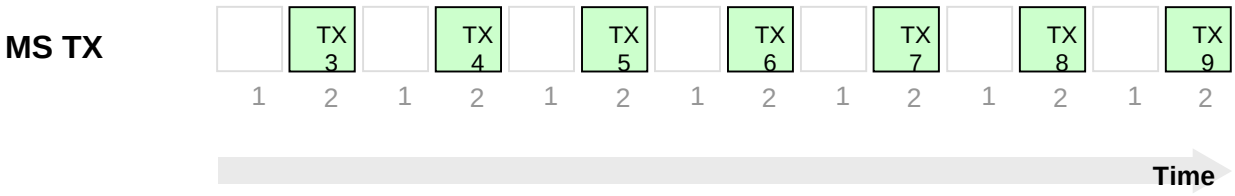


Figure 5.20: TDMA direct mode timing

5.1.5 Reverse Channel (RC) timing

5.1.5.0 Reverse Channel (RC) timing - Introduction

In order to support certain facilities, both the BS and MS units may send RC signalling back to a source while it is transmitting. The following RCs signalling are defined:

- Embedded RC signalling;
- Dedicated RC signalling; and
- Standalone RC signalling.

Embedded and Dedicated RC signalling is used for the outbound channel, the Standalone RC signalling is used for the inbound channel and direct mode.

Embedded RC signalling has the benefit of using only small amounts of bandwidth but is slow since the fields set aside for RC are widely spaced. Dedicated RC signalling has the benefit of fast response since an entire channel is set aside for this purpose but supports only a single call on an RF channel.

5.1.5.1 Embedded outbound Reverse Channel (RC)

Embedded RC signalling utilizes the 48-bit field defined for the centre of the burst in order to provide RC information. This type of channel may be available both in 1:1-mode and 2:1-mode of operation.

On the outbound path, embedded RC information is carried on the alternate channel of the intended target MS. For example, calls using outbound channel 2 for traffic will use outbound channel 1 for RC information.

The following rules apply to sending outbound RC information:

- An RC is sent in place of outbound voice burst F embedded LC during voice packets.

- An RC in not sent in a voice header or data header, but can be sent in a UDT data header.
- An RC is not sent in the first burst following a voice transmission (typically a voice terminator burst).
- Subsequent/repeated RC messages shall occur no sooner than 360 ms after the previous RC message. (Example would be during data continuation bursts.)

Figure 5.21 illustrates an example of the fastest (360 ms) subsequent/repeated RC timing and access in the aligned channel timing mode. The bursts in outbound channel 1, which carry the traffic for call "A", contain SYNC or embedded signalling data as dictated by the content of call A except for every 6th burst which carries the RC information for call "B" when appropriate. The MSs receiving call "B" listen to outbound channel 2 for their traffic and channel 1 for RC information. This arrangement allows the transmitter for call B to receive RC information without interrupting its transmission as shown in figure 5.21.

NOTE: This method of RC signalling requires the use of aligned traffic channels.

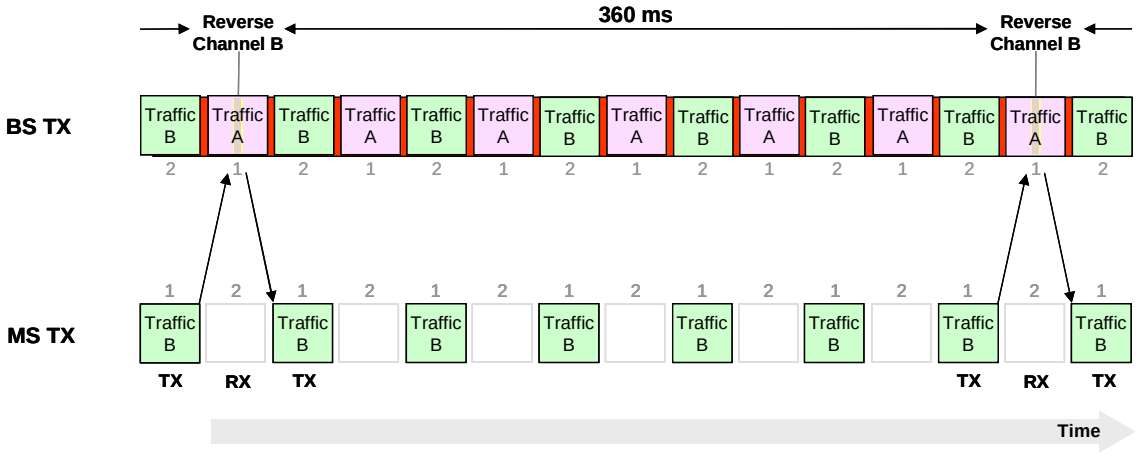


Figure 5.21: Embedded outbound Reverse Channel (RC) timing

5.1.5.2 Dedicated outbound Reverse Channel (RC)

For Dedicated RC signalling, one outbound channel shall be used for voice/data traffic while the other outbound channel may be used for RC signalling. This type of channel may be available only in a 1:1-mode of operation.

The RC information is carried in the 48-bit embedded field of a general data burst as it was for the embedded RC. However, every burst on the secondary channel carries either RC information or a SYNC pattern embedded within an Idle message. The mix of RC bursts and SYNC bursts can be changed dynamically by the BS based on perceived instantaneous needs. The mix can vary from all SYNC pattern to all RC signalling and anywhere in between.

Figure 5.22 illustrates an example of RC timing and access.

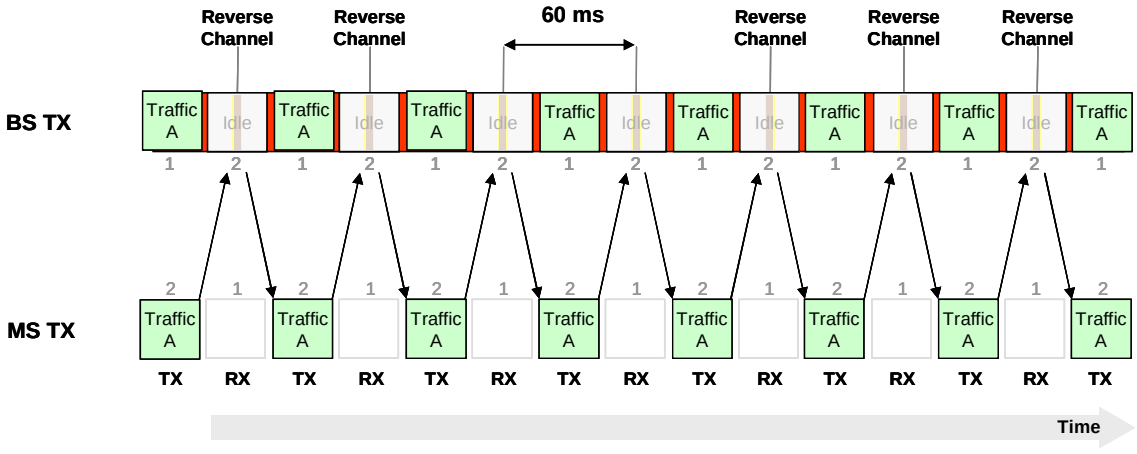


Figure 5.22: Dedicated outbound Reverse Channel (RC) timing

The bursts in outbound channel 1 carry the traffic for call "A". The bursts in outbound channel 2 contain either SYNC or RC signalling within an Idle burst. When required, this arrangement can deliver RC information every 60 ms. Figure 5.22 shows how the transmitter for call "A" can transition after every inbound burst to the outbound channel, recover the RC, and transition back to the inbound transmission.

5.1.5.3 Standalone inbound Reverse Channel (RC)

Inbound standalone RC bursts may be used by MSs that want to generate RC signalling. One inbound channel shall be used for voice or data traffic while the other inbound channel shall be used for RC signalling. This type of channel may be available only in a 1:1-mode of operation. The shortened nature of the standalone burst allows the MS to transition from receiving an outbound burst to transmitting an inbound standalone RC burst and back to receiving an outbound burst.

Figure 5.23 illustrates an example of RC timing and access.

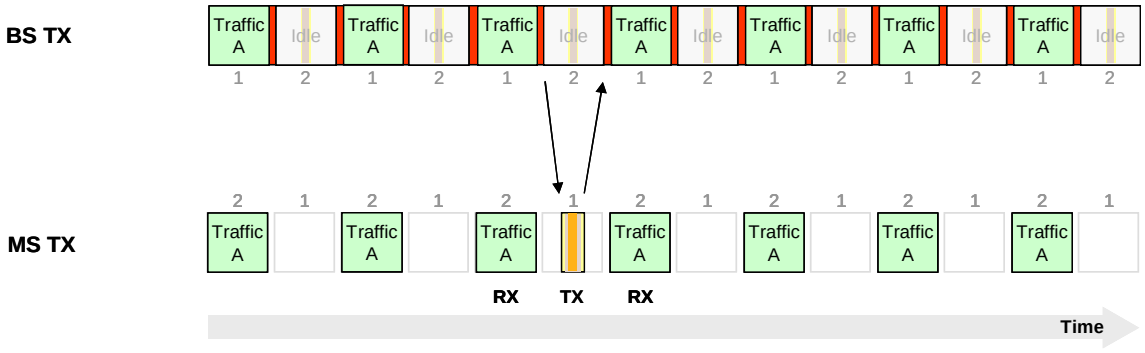


Figure 5.23: Standalone inbound Reverse Channel (RC) timing

The bursts in inbound channel 2 carry the traffic for call "A". The bursts in inbound channel 1 are unused except for the instance of a standalone RC burst that is shown.

5.1.5.4 Direct mode Reverse Channel (RC)

RC signalling may be used in direct mode to allow the receiver to signal the transmitter during a voice/data call without either party missing information.

NOTE: RC signalling applies only to Tier II and Tier III products.

In direct mode, one burst of the TDMA channel shall be used as the forward path for traffic while the other burst (on the same RF frequency) shall be used as the reverse path for RC signalling.

Figure 5.24 illustrates RC signalling that is sent directly to a transmitting MS.

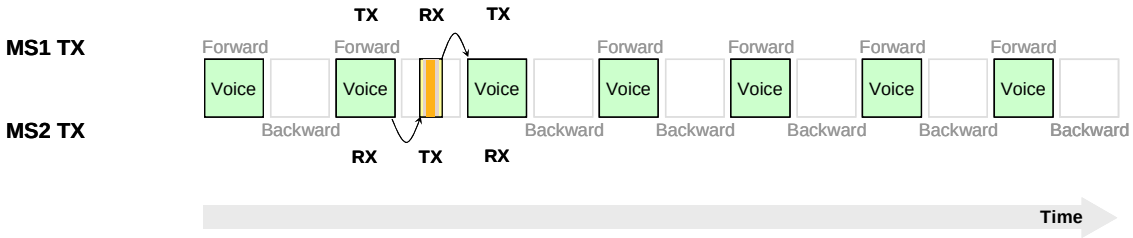


Figure 5.24: Direct mode Reverse Channel (RC) timing

A standalone RC burst shall be used that contains both SYNC and signalling. The arrows in figure 5.24 indicate where the transmitting MS shall transition to receive the RC signal and transition back to the transmit mode. The receiving MS shall follow the same transitions from receiving the traffic to transmitting the RC burst and back to receive.

5.2 Channel access

5.2.0 Channel access - Introduction

This clause describes the Tier II and Tier III products channel access rules and procedures that MS units shall use to conform to when transmitting both on two frequency BS and single frequency (bi-directional) channels. These channel access accommodate different levels of MS "politeness" (e.g. Listen Before Transmit (LBT)) and take account of co-existence with analogue activity and other digital protocols on the same RF carrier.

Tier I products channel access may use LBT channel access rules.

This clause also describes how BSs are able to restrict channel access while activity is present (or expected) on their inbound channels and during call hang time periods. However, it should be noted that there is a wide degree of flexibility for the way in which BSs may regulate channel access, thereby allowing different BS implementations to restrict channel access according to their particular system requirements.

Figure 5.25 illustrates the following three use cases for a two frequency BS channel consisting of an outbound channel and an inbound channel:

Use Case 1: Either for two independent "repeated" simplex calls, two independent "MS to fixed end" duplex calls or a single "repeated" duplex call.

Use Case 2: Either for a single "repeated" simplex call or a single "MS to fixed end" duplex call.

Use Case 3: For a single "repeated" simplex call with RC.

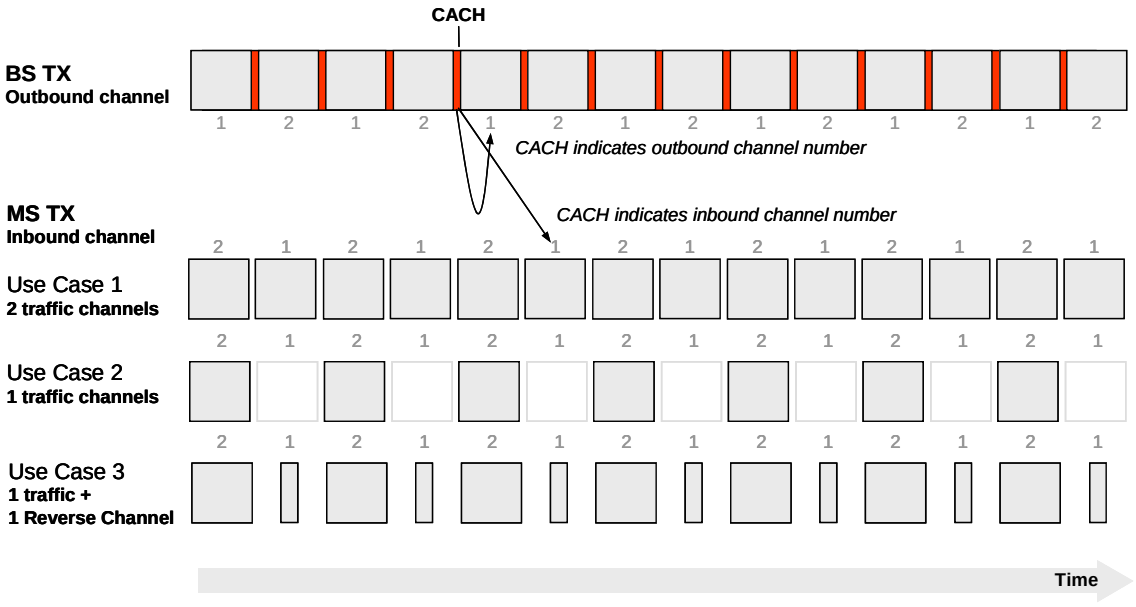


Figure 5.25: Two frequency BS channel

Figure 5.26 illustrates the following five use cases for a single frequency bi-directional channel:

Use Case 1: Either for a "direct" duplex call or a single frequency "repeated" simplex call.

Use Case 2: For a "direct" simplex call.

Use Case 3: For a "direct" simplex call with RC.

Use Case 4: For a TDMA "direct" simplex call.

Use Case 5: For two independent TDMA "direct" simplex calls.

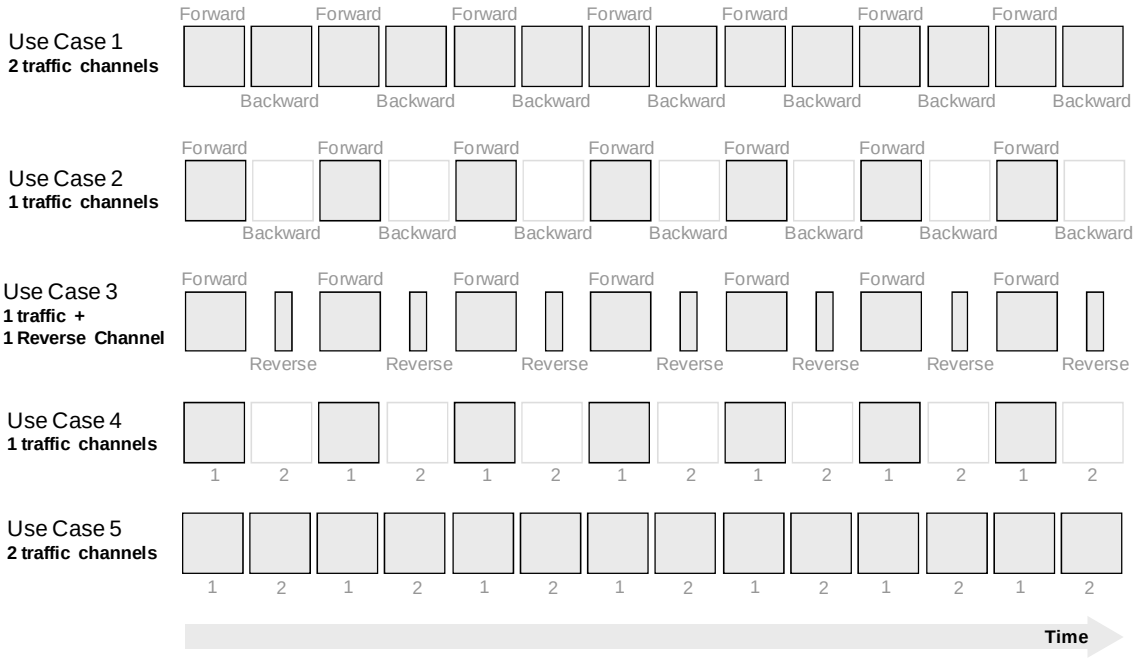


Figure 5.26: Single frequency (bi-directional) channel

5.2.1 Basic channel access rules

5.2.1.1 Types of channel activity

When accessing a channel to transmit, a DMR entity (MS or BS) shall take account of the following types of activity which may already be present on the channel:

- DMR activity;
- other digital protocol activity (see notes 1 and 2);
- analogue activity (see note 1).

NOTE 1: DMR entities are able to coexist with non-DMR entities.

NOTE 2: DMR entities employing the 2-slot TDMA protocol are not expected to coexist on the same channels as DMR entities employing the continuous transmission mode protocol.

When determining whether activity is present on a repeater mode or direct mode channel, a DMR entity shall monitor the RSSI level. If after a maximum period of time T_ChMonTo the RSSI level has not exceeded a configurable threshold N_RssiLo, then the DMR entity shall assume that activity is not present on the channel (see note 3). If however the RSSI level does exceed threshold, then the DMR entity shall assume that activity is present on the channel and it shall attempt to become frame synchronized to the activity for specific channel access policies, as defined in later clauses of the present document. If the DMR entity is successful in becoming frame synchronized to the activity, then the DMR entity shall assume that DMR activity is present on the channel. If however after a maximum period of time T_ChSyncTo the DMR entity has not become frame synchronized to the activity, then the MS shall assume that the activity is non-DMR activity.

NOTE 3: DMR entities may employ different N_RssiLo values for different channel access policies.

When determining whether activity is present on a TDMA direct mode channel for channel access, a DMR entity shall monitor the RSSI level and search for TDMA direct mode synchronization patterns. If after a maximum period of time T_ChMonTo the RSSI level has not exceeded a configurable threshold N_RssiLo, then the DMR entity shall assume that activity is not present on the channel. However, if a TDMA direct mode synchronization pattern is detected, the MS shall synchronize. This is to ensure the current channel slot timing is used if access is granted.

5.2.1.2 Channel status

For single frequency channels, while no activity is present the channel shall be considered "Idle" (CS_Idle). For non-TDMA direct mode single frequency channels, while activity is present (either DMR or otherwise) the channel shall be considered "Busy" (CS_Busy). For TDMA direct mode single frequency channels, while activity is present in a time slot the time slot shall be considered "Busy" (CS_Busy) and while no activity is present in a time slot, the time slot shall be considered "Idle" (CS_Idle).

For two frequency BS channels, while no activity is present on the outbound channel, MSs shall consider the inbound channel to be "Idle" and while non-DMR activity is present on the outbound channel, MS shall consider the inbound channel to be "Busy".

5.2.1.3 Timing master

For two frequency BS channels if a BS is active and transmitting its outbound channel, the timing master shall be the BS and MSs shall derive slot timing by monitoring the outbound channel and becoming frame synchronized to the outbound channel activity. The one exception to this rule shall be where a MS fails to detect outbound channel activity in which case it shall assume the BS to be inactive.

Where this is the case and the MS wants to use "Repeater Mode BS established timing", the MS shall be permitted to transmit asynchronous "BS activation" signalling to the BS in accordance with the "BS activation" feature (described in ETSI TS 102 361-2 [5]). On becoming activated, the BS shall commence transmitting activity on the outbound channel and the MS shall derive slot timing from this activity.

Where BS is able to initiate transmitting on the outbound channel without decoding "BS activation" signalling, but by means of decoding any correct uplink activity, the MS shall be permitted to use "Repeater Mode MS established timing". In this case the BS acts in such way that the MS inbound channel is frame synchronized to the outbound one.

For direct channels there is no timing master and MSs shall be permitted to transmit asynchronously. The one exception to this rule shall be where a MS wishes to transmit in a reverse slot in which case it shall derive slot timing by monitoring the forward slots and becoming frame synchronized to the channel activity in the forward slots.

In TDMA direct mode, an elected channel timing leader MS shall establish the timing reference for both time slots on the frequency. MS units that are not the channel timing leader are responsible for retransmitting the timing reference out to the edge of the wide area system. This mechanism helps to insure that all MS units in the wide area system are working from the same timing reference. In general a MS transmits in the appropriate slot with the channel slot timing established by the channel timing leader MS.

5.2.1.4 Hang time messages and timers

A voice call shall consist of a series of speech items separated by gaps known as "call hang time periods". Also, for two frequency BS channels, as soon as this call hang time period expires the BS may optionally remain active for a period of time known as the "channel hang time period".

For two frequency BS channels, the call hang time period T_CallHt (which may be zero) shall be determined by the BS configuration and during this period of time the BS shall maintain the channel in the "Busy" state by transmitting Terminator with LC (hang time) messages on the outbound channel (with the source and destination IDs set to reflect the voice call in progress) and setting the AT bit to "Busy". MSs employing a "polite" level of politeness (see clause 5.2.1.6) shall not be permitted to transmit on the "Busy" channel unless they are either participating in the specified voice call or they are employing the "polite to own Colour Code" level of politeness (see clause 5.2.1.6) and their Colour Code is different to that contained in the hang time messages (see note). As soon as the call hang time period T_CallHt expires, the channel hang time period T_ChHt may optionally commence and during this period of time the BS shall maintain the channel in CS_Idle state by setting the status bit to "Idle".

NOTE: If the Colour Code is different, then the hang time messages will be considered co-channel interference from another site.

5.2.1.5 Slot 1 and 2 dependency

If a system is configured for 2:1-mode of operation, then both inbound slots shall be available for traffic and the "Busy" status for each inbound slot shall be independently controlled. For example, a voice or data call may be in progress on one slot while the other slot is "Idle".

If a system is configured for 1:1-mode of operation and the dual slot data capability is used, then both inbound slot 1 and 2 shall be used for traffic. The BS shall be able to set the status of each inbound slot to "Busy" or "Idle" according to the incoming slots.

In all other cases of a system is configured for 1:1-mode of operation, then inbound slot 2 shall be used for traffic and inbound slot 1 may provide the optional inbound RC signalling opportunities. The BS shall be able to set the status of each inbound RC signalling opportunity to CS_Busy or CS_Idle. When set to CS_Busy, an inbound RC opportunity shall only be available to those MSs participating in the call in progress and when set to CS_Idle, an inbound RC opportunity shall be available to all MSs.

5.2.1.6 Transmit admit criteria

Where a MS has been solicited to transmit a response, it may transmit the response in the expected time slot irrespective of whether the channel is CS_Idle or CS_Busy. Additionally, while a MS is partied to a voice call, it may transmit irrespective of whether the channel is CS_Idle or CS_Busy with DMR activity pertaining to the same voice call. However, for all other situations, subscribers shall be configurable to employ the following levels of "politeness" on a channel:

- **Polite to all:** The MS shall refrain from transmitting on a channel while the channel state is CS_Busy with other activity (either DMR or otherwise).
- **Polite to own Colour Code:** The MS shall refrain from transmitting on the logical channel while the channel state is CS_Busy with other DMR activity containing the MS's own (see note) Colour Code. For all other types of activity (including DMR activity containing a different Colour Code) already present on the channel, the MS shall transmit regardless.
- **Impolite:** The MS shall transmit on a channel regardless of any other activity (either DMR or otherwise) already present on the channel.

NOTE: This refers to the Colour Code (CC) that the MS intends embedding in its own transmission.

On a given channel, not all features may be supported the same level of politeness. So for example, voice transmissions may be configured to be "impolite" while packet data transmissions are configured to be "polite". Details of which levels of politeness are employed by which facilities are contained in ETSI TS 102 361-2 [5].

5.2.1.7 Transmission re-tries

Certain transmissions solicit responses and where these responses are not received (e.g. due to collisions, interference, etc.) the transmitting entity may repeat the original transmission a number of times either until the response is received or the transmitting entity gives up.

For two frequency BS channels, a MS transmitting a message that requires a response from the BS shall wait for a configurable number of slots for the response (this configuration parameter shall allow for different system delays). However, a BS transmitting a message that requires a response from a MS shall expect to receive the response within a configurable number of slots (see note 1).

NOTE 1: The waiting times for re-transmission and the maximum number of re-tries are defined facility-by-facility basis in ETSI TS 102 361-2 [5].

For single frequency (bi-directional) channels (see note 2), a DMR entity (MS or BS) transmitting a message that requires a response from another DMR entity expect to receive the response in the next but one slot.

NOTE 2: This refers to direct channels.

In all cases, if a response is not received within the expected number of slots, then the DMR entity shall repeat the message a number of times (each time waiting for a response) either until a response is received, the message has been repeated a maximum number of times or unexpected DMR activity is detected (i.e. DMR activity not related to the original message). If a response is eventually received, the procedure shall have concluded successfully, otherwise if no response is received or unexpected DMR activity is detected, then the procedure shall have failed (see note 3).

NOTE 3: Where unexpected DMR activity is detected, certain facilities (e.g. data) may require a random back-off and re-try procedure.

5.2.2 Channel access procedure

5.2.2.0 Channel access procedure - Introduction

The basic channel access rules are given in clause 5.2.1 of the present document. This clause expands upon these rules and uses informative SDL diagrams where necessary to illustrate and highlight specific points in direct mode, TDMA direct mode and repeater mode. Direct, TDMA direct and repeater modes support impolite, polite to own colour code and polite to all channel access mechanisms. Repeater mode also supports a BS outbound activation mechanism that is initiated by the MS.

The different MS high level states as defined in annex G are used as the starting MS states when a transmission is requested. Channel access can also be requested from the Out_of_Sync_Channel_Monitored state (PS_OutOfSyncChMon), which is a substate of the Out_of_Sync state (PS_OutOfSync). For non-time critical applications the MS may also transition to the Holdoff state (PS_Holdoff) while waiting for the channel to become CS_Idle. These states are defined below:

- **Out_of_Sync_Channel_Monitored (PS_OutOfSyncChMon):** An MS transitions to this state from PS_OutOfSync after it has been monitoring the RF level and has not found SYNC for a duration of time long enough to establish knowledge of the channel. This time limit is established by the Monitor timer T_Monitor. After the expiration of this timer the MS has determined the channel is idle with respect to DMR activity. In this state the MS continues to monitor the RF level and search for SYNC.

- **Holdoff (PS_Holdoff):** An MS transitions to this state when a non-time critical transmission is requested and the channel is busy. Here the transmission request is queued by the MS. If a random holdoff is required the MS starts a random holdoff timer T_Holdoff. The services that allow a transmission to enter this state are defined in ETSI TS 102 361-2 [5].

NOTE: T_Holdoff is started for non-time critical transmissions.

5.2.2.1 Direct mode Channel Access

5.2.2.1.0 Direct mode Channel Access - Introduction

In direct mode it is possible to initiate channel access from any of the high level MS states as defined in annex G. These high level states include PS_OutOfSync, PS_InSyncUnknownSystem, PS_NotInCall and PS_OthersCall or PS_MyCall. It is also possible to request channel access while in PS_OutOfSyncChMon.

5.2.2.1.1 MS Out_of_Sync Channel Access

The three access mechanisms from the High Level MS Out_of_Sync state are illustrated in figure 5.27. This is an informative SDL diagram that generically shows transmission request from the Out_of_Sync state. In the Out_of_Sync state the MS has not resided on the channel long enough to immediately know the status of the channel. Therefore it shall attempt to qualify the channel status. Additionally for completeness, figure 5.27 shows how transitions from Out_of_Sync state to either Out_of_Sync_Channel_Monitored or In_Sync_Unknown_System states occur. States not defined in the MS High Level SDL sections are Out_of_Sync_Find_Sync and In_Sync_Unknown_System_Find_CC. These are defined below:

- **Out_of_Sync_Find_Sync:** After a MS has determined RF is present on the channel it transitions to this state and attempts to synchronize to the signal. Expiration of the Monitor Timer T_Monitor while in this state implies the channel activity is non-DMR. For simplicity, this is illustrated as Find_Sync in figure 5.27.

- **In_Sync_Unknown_System_Find_CC:** After a MS has synchronized to the channel it transitions to this state and attempts to decode the Colour Code present on the channel. Expiration of the TX_CC_Timer (T_TxCC) while in this state implies the channel activity is for a different system. For simplicity, this is illustrated as Find_CC in figure 5.27.

A transmission request employing impolite channel access from the High Level MS Out_of_Sync state is always granted.

A transmission request employing either type of polite channel access policy from the High Level Out_of_Sync state will first measure the RF level present on the channel. If the measured RF level is less than the programmed RF threshold, then the transmission is granted for either polite access policy (see note). If the measured RF level is greater than or equal to the programmed N_RssiLo and the requested polite channel access type is polite to all, the MS yields to the current channel activity and denies the transmission or places it in queue.

NOTE: DMR entities may employ different N_RssiLo values for different channel access policies.

If the measured RF level is greater than or equal to the programmed N_RssiLo, the requested polite channel access type is polite to own Colour Code and the Monitor Timer T_Monitor has not expired the MS attempts to synchronize to the current channel activity. If the Monitor Timer T_Monitor expires the MS assumes the channel activity was a non-DMR transmission and the transmission is granted. If the MS is able to synchronize to the channel activity, then it starts the TX_CC_Timer (T_TxCC) and attempts to determine the Colour Code on the channel.

If the TX_CC_Timer (T_TxCC) expires or the Colour Code does not match, then the MS grants the transmission. If the Colour Code matches, then the transmission is denied or placed in queue and the MS moves to the High Level Not_in_Call state.

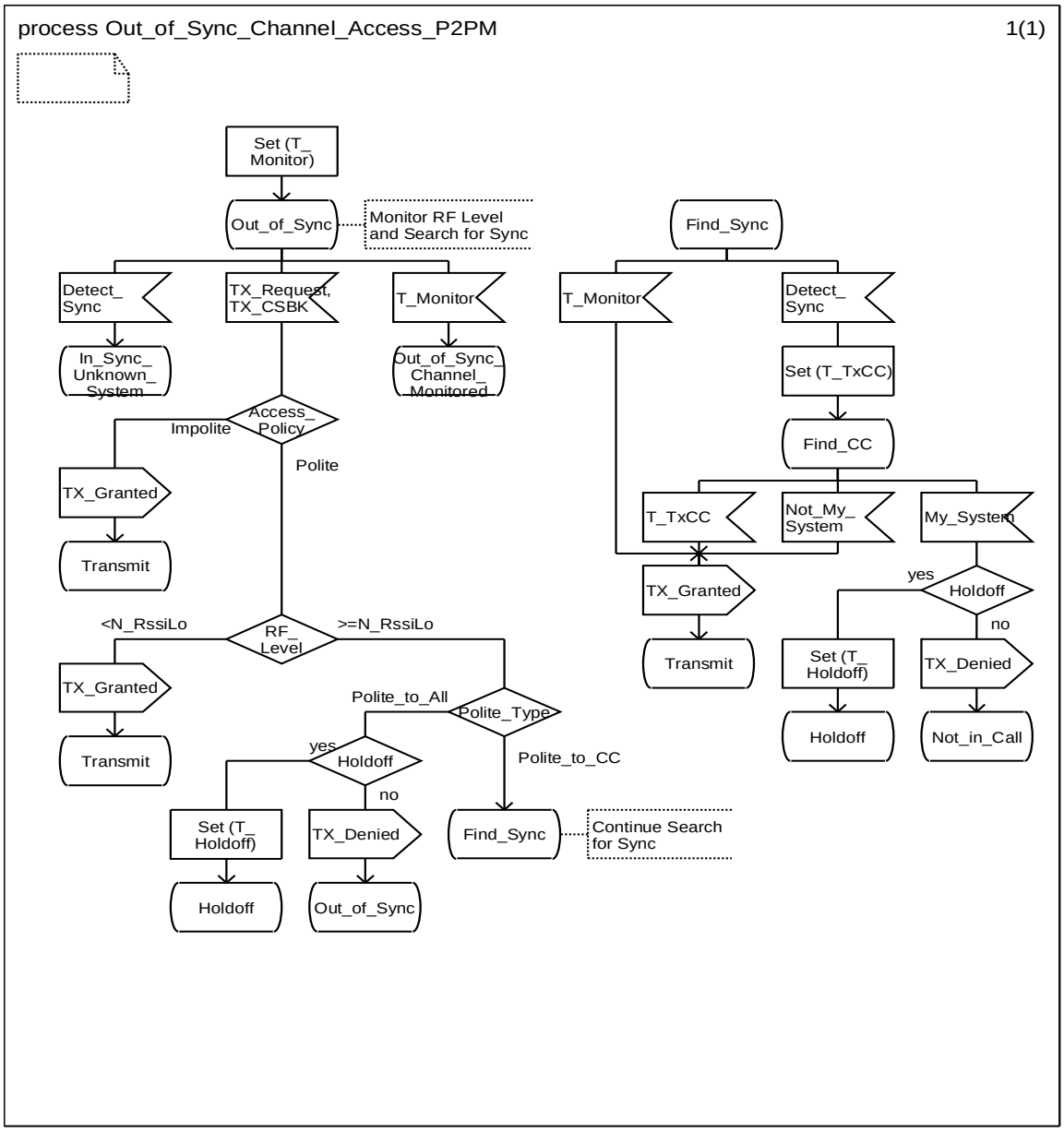


Figure 5.27: Out_of_Sync SDL diagram

5.2.2.1.2 MS Out_of_Sync_Channel_Monitored Channel Access

The three access mechanisms from the Out_of_Sync_Channel_Monitored state are illustrated in figure 5.28. This informative SDL diagram describes a transmission request when the MS knows the channel is currently idle with respect to DMR activity and also knows the RF level on the channel.

All transmissions from this state are granted except when the polite channel access type is polite to all and the RF level exceeds N_RssiLo. In this case the transmission is denied or placed in queue.

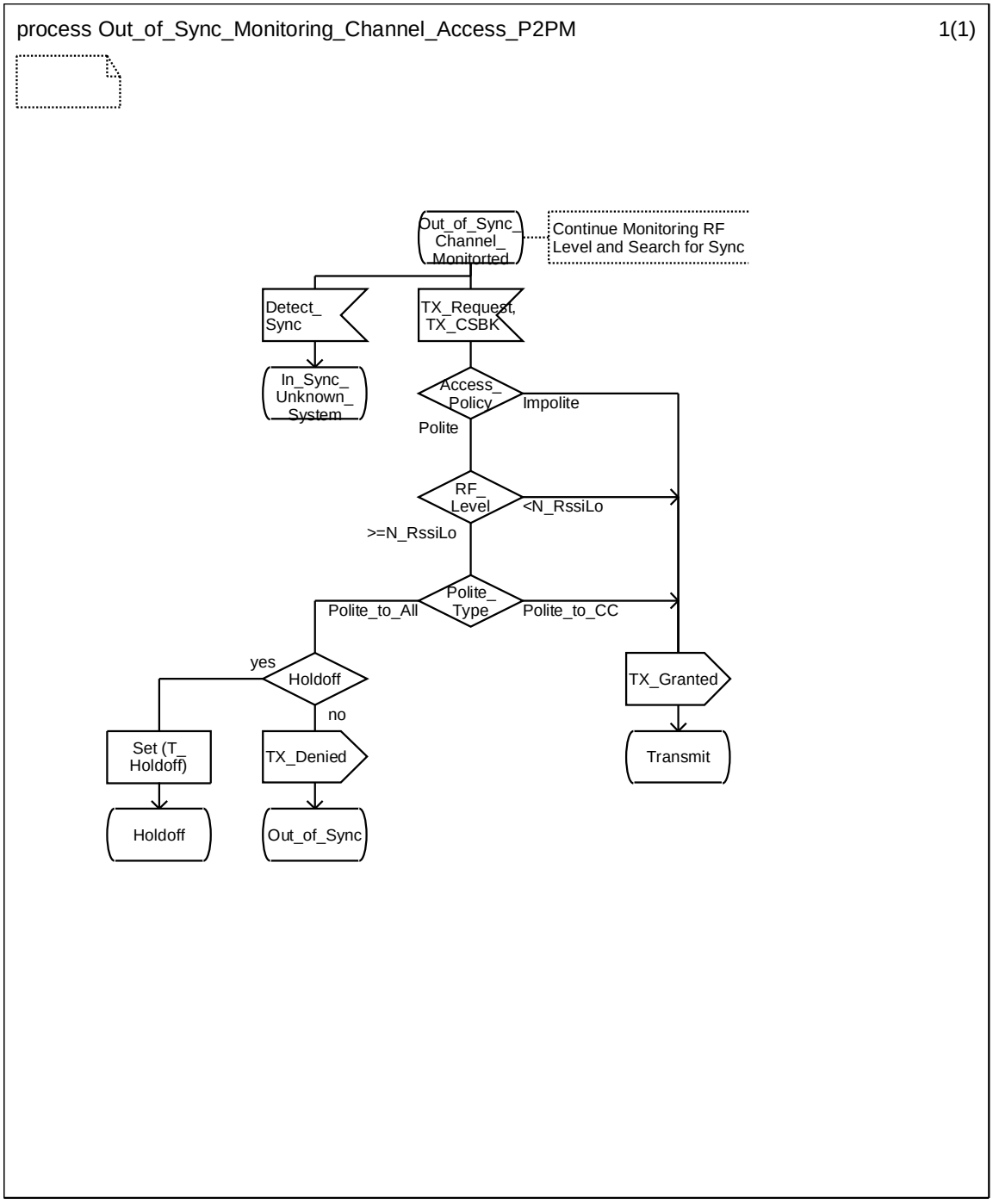


Figure 5.28: Out_of_Sync_Channel_Monitored SDL diagram

5.2.2.1.3 MS In_Sync_Unknown_System Channel Access

The three access mechanisms from the High Level MS In_Sync_Unknown_System state are illustrated in figure 5.29.

A transmission request employing impolite channel access policy from the High Level MS In_Sync_Unknown_System state is always granted.

A transmission request employing a polite channel access type of polite to all from the High Level In_Sync_Unknown_System state will deny the transmission or place in queue. Here the MS yields to the current channel activity.

A transmission request employing a polite channel access type of polite to own Colour Code from the High Level MS In_Sync_Unknown_System will start the TX_CC_Timer (T_TxCC). Here the MS attempts to determine the Colour Code on the channel. From this point the channel access is the same as from this point when channel access is requested from the High Level Out_of_Sync state.

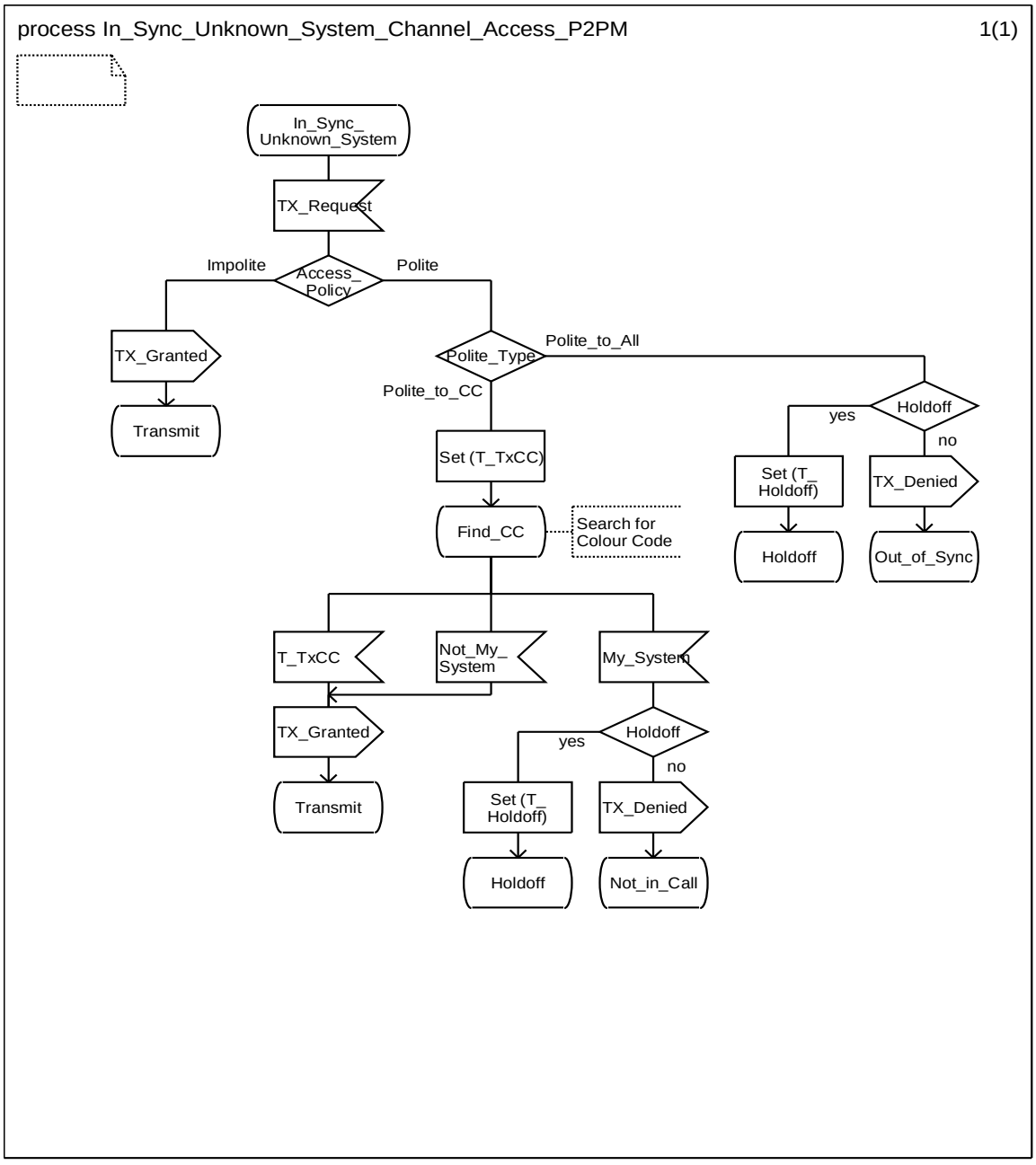


Figure 5.29: In_Sync_Unknown_System SDL diagram

5.2.2.1.4 MS Not_in_Call Channel Access

A transmission request employing impolite channel access policy from the High Level MS Not_in_Call state is always granted.

A transmission request employing either polite channel access policy type from the High Level Not_in_Call state will be denied or placed in queue if it is non-time critical. This occurs since in order to reach this state the MS has matched the Colour Code. The MS will stay in the Not_in_Call state.

5.2.2.1.5 MS Others_Call Channel Access

A transmission request employing impolite channel access policy from the High Level MS Others_Call state is always granted.

A transmission request employing either polite channel access policy type from the High Level Others_Call state will be denied or placed in queue if it is non-time critical. This occurs since in order to reach this state the MS has matched the Colour Code. The MS will stay in the Others_Call state.

5.2.2.1.6 MS My_Call Channel Access

In this state the MS is party to the call and will use the impolite channel access method. This is regardless of the programmed channel access policy programmed into the MS.

5.2.2.2 Repeater mode channel access

5.2.2.2.0 Repeater mode channel access- Introduction

In repeater mode it is possible to initiate channel access from any of the high level MS states as defined in annex G. These high level states include Out_of_Sync, In_Sync_Unknown_System, Not_in_Call and Others_Call, In_Session or My_Call. It is also possible to request channel access while in the Out_of_Sync_Channel_Monitored state. When a transmission request occurs from the Out_of_Sync, or In_Sync_Unknown_System states, the MS shall first verify that the outbound is present. If it is not present, the MS attempts to activate the BS outbound.

5.2.2.2.1 MS Out_of_Sync Channel Access

In repeater mode channel activity is not sufficient to grant a MS transmission from the High Level Out_of_Sync state. The MS shall first sync to the outbound, match the Colour Code and determine the slotting structure. The three access mechanisms from the Out_of_Sync state are illustrated in figure 5.30. This is an informative SDL diagram that generically shows transmission requests from the Out_of_Sync state. In the Out_of_Sync state the MS has not resided on the channel long enough to immediately know the status of the channel. Therefore it shall attempt to qualify the channel status. Additionally for completeness, figure 5.30 shows how transitions from Out_of_Sync state to either Out_of_Sync_Channel_Monitored or In_Sync_Unknown_System states occur. States not defined in the MS High Level SDL sections or the direct mode channel access section are TX_Wakeup_Message and In_Sync_Unknown_System_Find_CC_Slot. These are defined below:

- **TX_Wakeup_Message:** After a MS has determined that the correct BS outbound is not present, it transitions to this state and transmits a burst to activate the BS outbound.

- **In_Sync_Unknown_System_Find_CC_Slot:** After a MS has synchronized to the channel it transitions to this state and attempts to decode the Colour Code present on the channel and the slotting structure of the channel. Expiration of the TX_CC_Slot_Timer (T_TxCCSlot) while in this state implies the channel activity is for a different system.

No matter which channel access mechanism is desired from this state, the MS sets the Wakeup_Message counter to zero. If the measured RF level is less than the programmed RF threshold N_RssiLo, the MS transitions to the TX_Wakeup_Message state. Details on the TX_Wakeup_Message state are given in figure 5.33. If the measured RF level is greater than or equal to the programmed RF threshold N_RssiLo then the MS transitions to Find_Sync and attempts to acquire synchronization.

If the Monitor Timer T_Monitor expires, it is assumed the channel activity was non-DMR. If the channel access policy is impolite or the polite policy type is polite to own Colour Code the MS transitions to the TX_Wakeup_Message state.

If SYNC is detected, the MS starts the TX_CC_Slot_Timer (T_TxCCSlot) and attempts to determine the Colour Code and slotting structure of the received signal. If the timer expires, then the MS transitions to the TX_Wakeup_Message state. If the Colour Code does not match, the MS denies or queues the transmission if the polite channel access type is polite to all or transitions to the TX Wakeup_Message state if the channel access policy is impolite or the polite policy type is polite to own Colour Code. If the MS matches its Colour Code and determines the slotting structure, the MS moves to the High Level In_Sync_My_System state. Transmissions from this state are defined in clause 5.2.2.2.5.

If the MS arrives at the Find_Sync state from the TX_Wakeup_Message state, a Sync_WU_Timer (T_SyncWu) has been started. If this timer expires, the MS transitions back to the TX_Wakeup_Message state.

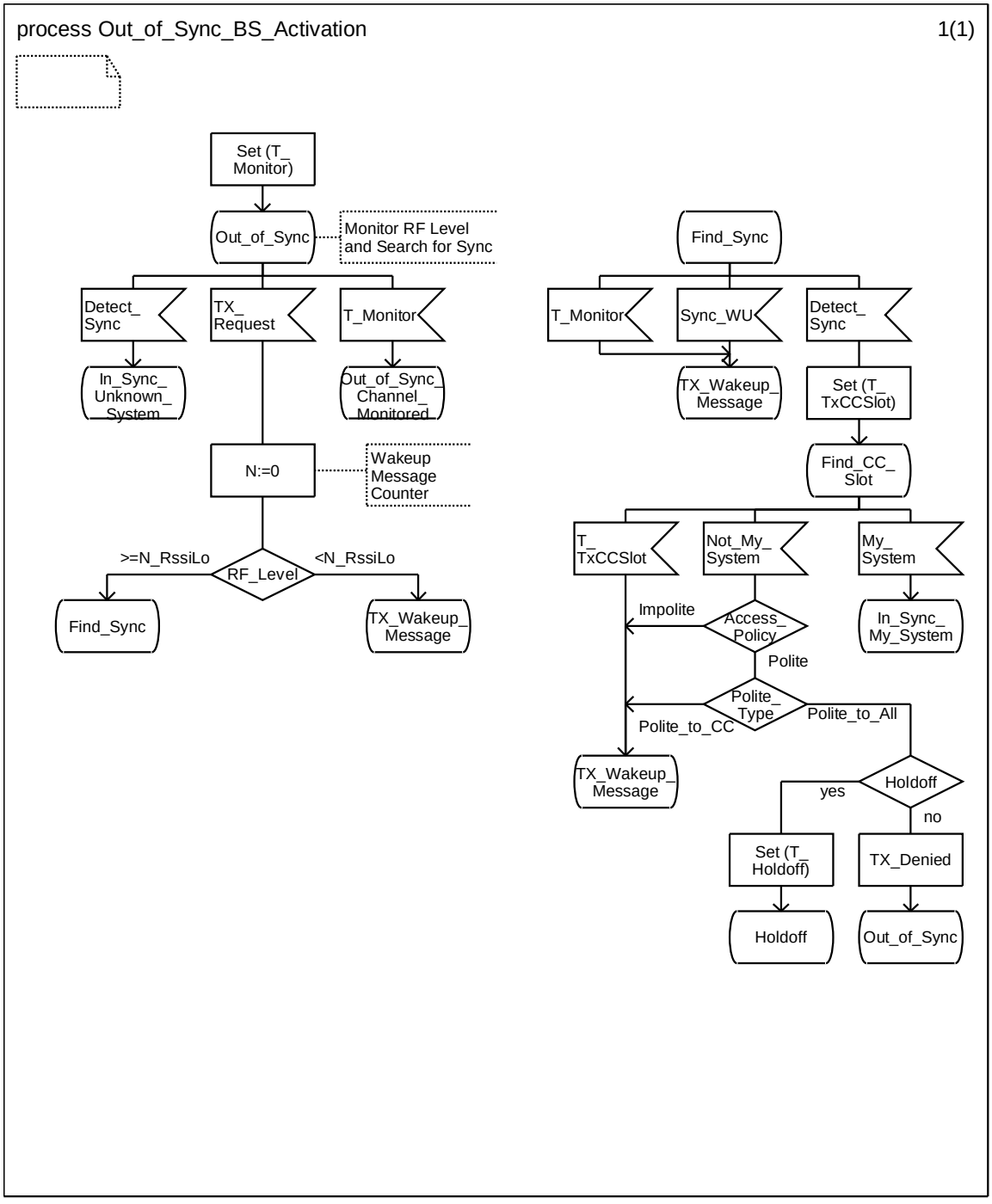


Figure 5.30: Out_of_Sync SDL diagram

5.2.2.2.2 MS Out_of_Sync_Channel_Monitored Channel Access

The three access mechanisms from the Out_of_Sync_Channel_Monitored state are illustrated in figure 5.31. This informative SDL diagram describes a transmission request when the MS knows the channel is currently idle with respect to DMR activity and also knows the RF level on the channel.

Upon receiving the TX_Request primitive, the Wakeup Message Counter is initialized to zero. A transition to the TX_Wakeup_Message state always occurs except when the polite channel access type is polite to all and the RF Level exceeds the RF threshold N_RssiLo. In this case the transmission is either denied or placed in queue.

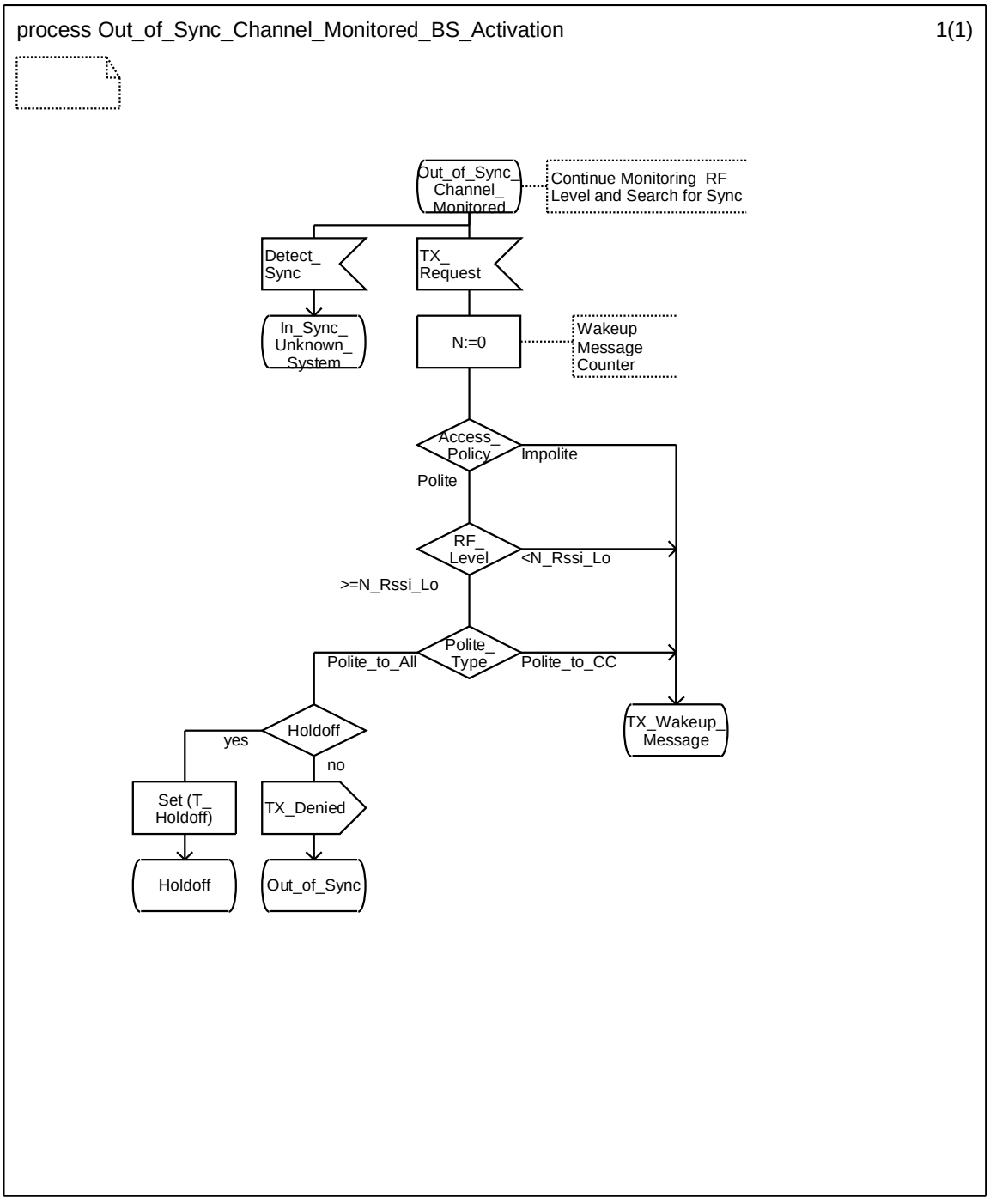


Figure 5.31: Out_of_Sync_Channel_Monitored channel access

5.2.2.2.3 MS In_Sync_Unknown_System channel access

When channel access is requested from the High Level In_Sync_Unknown_System state the MS sets the Wakeup_Message counter to zero and starts the TX_CC_Slot_Timer (T_TxCCSlot) while it attempts to determine the Colour Code and slotting structure of the received signal. If the MS matches its Colour Code and determines the slotting structure, the MS moves to the High Level Not_in_Call state. Transmissions from this state are defined in clause 5.2.2.2.5.

If the T_TxCCSlot expires or the Colour Code does not match and the channel access policy is impolite or the polite type is polite to Colour Code then the MS transitions to the TX_Wakeup_Message state. If the polite channel access type is polite to all then the transmission is either denied or placed in queue.

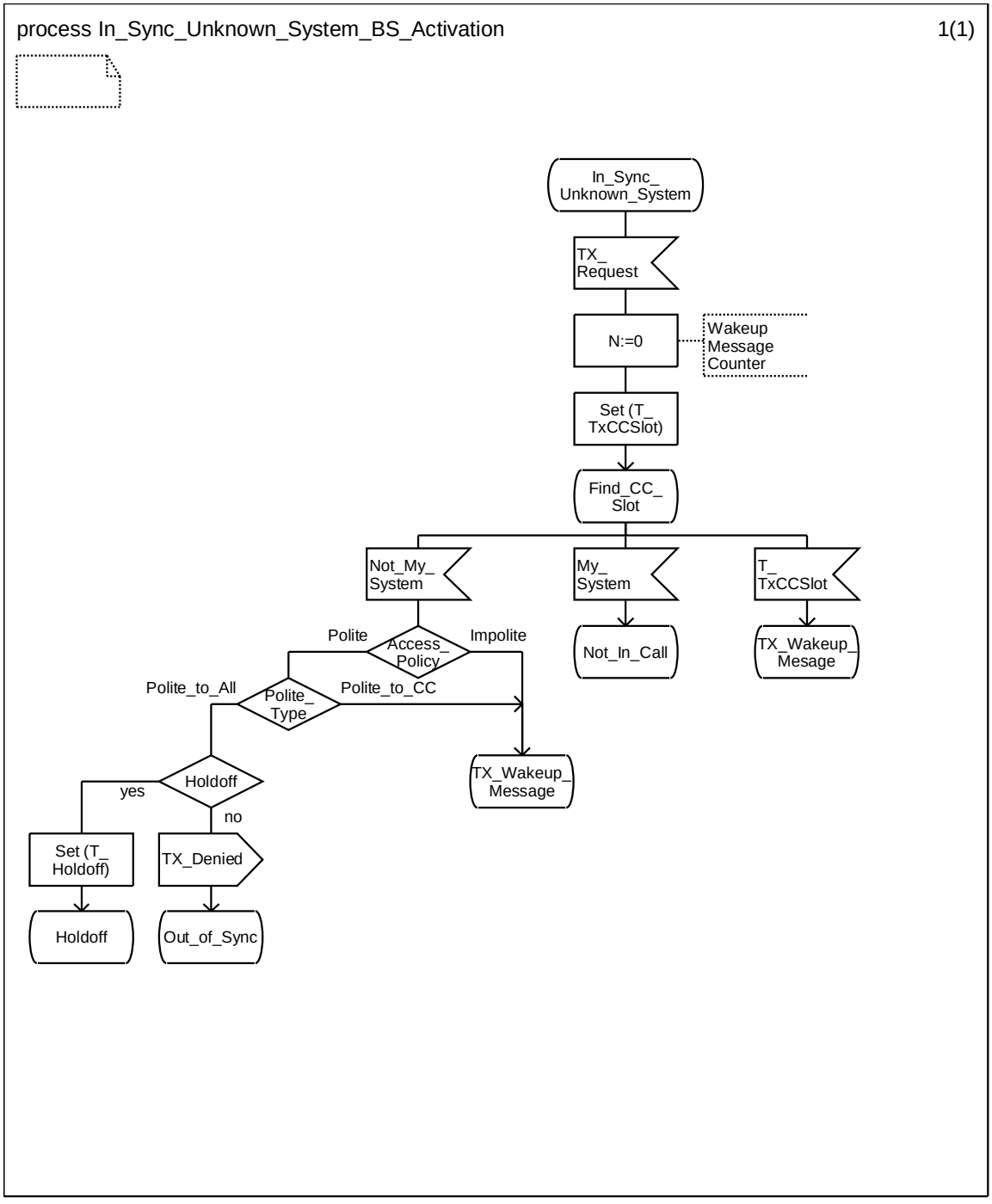


Figure 5.32: In_Sync_Unknown_System SDL diagram

5.2.2.2.4 MS TX_Wakeup_Message

A MS transitions to this state after a transmission is requested but the correct outbound has not been identified. The MS compares the programmable WU_Threshold N_Wakeup with the Wakeup Message counter. If the counter is equal to N_Wakeup, the number of wakeup attempts has been exhausted and the transmission is denied or queued. If the counter is less than N_Wakeup, the MS transmits a wakeup message, increments the Wakeup_Message counter by one and starts the Sync_WU_Timer (T_SyncWu). Then it transitions to the Find_Sync state.

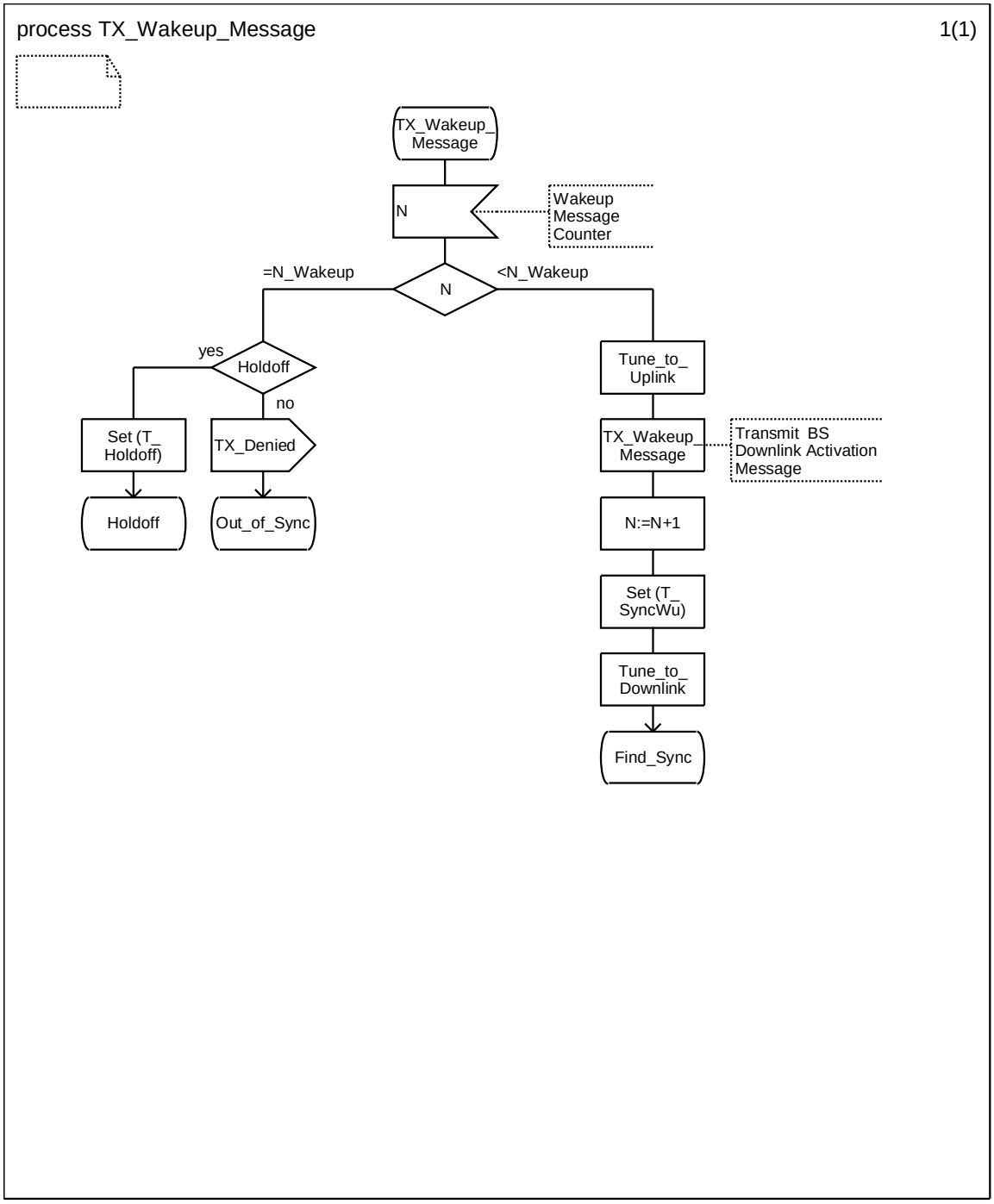


Figure 5.33: TX_Wakeup_Message SDL diagram

5.2.2.2.5 MS Not_In_Call channel access

The MS may be in this state when the TX_request is initiated or may transition to this state after successfully activating the BS outbound. Either way, an impolite channel access policy transmission is granted and a polite channel access type transmission shall first determine if the desired slot is idle. If the channel access policy is polite, the MS starts an Idle_Search_Timer (T_IdleSrch). If the Idle_Search_Timer (T_IdleSrch) expires before the channel is determined to be idle or the channel is determined to be busy the transmission is denied or queued. If the slot is determined to be idle the MS grants the transmission.

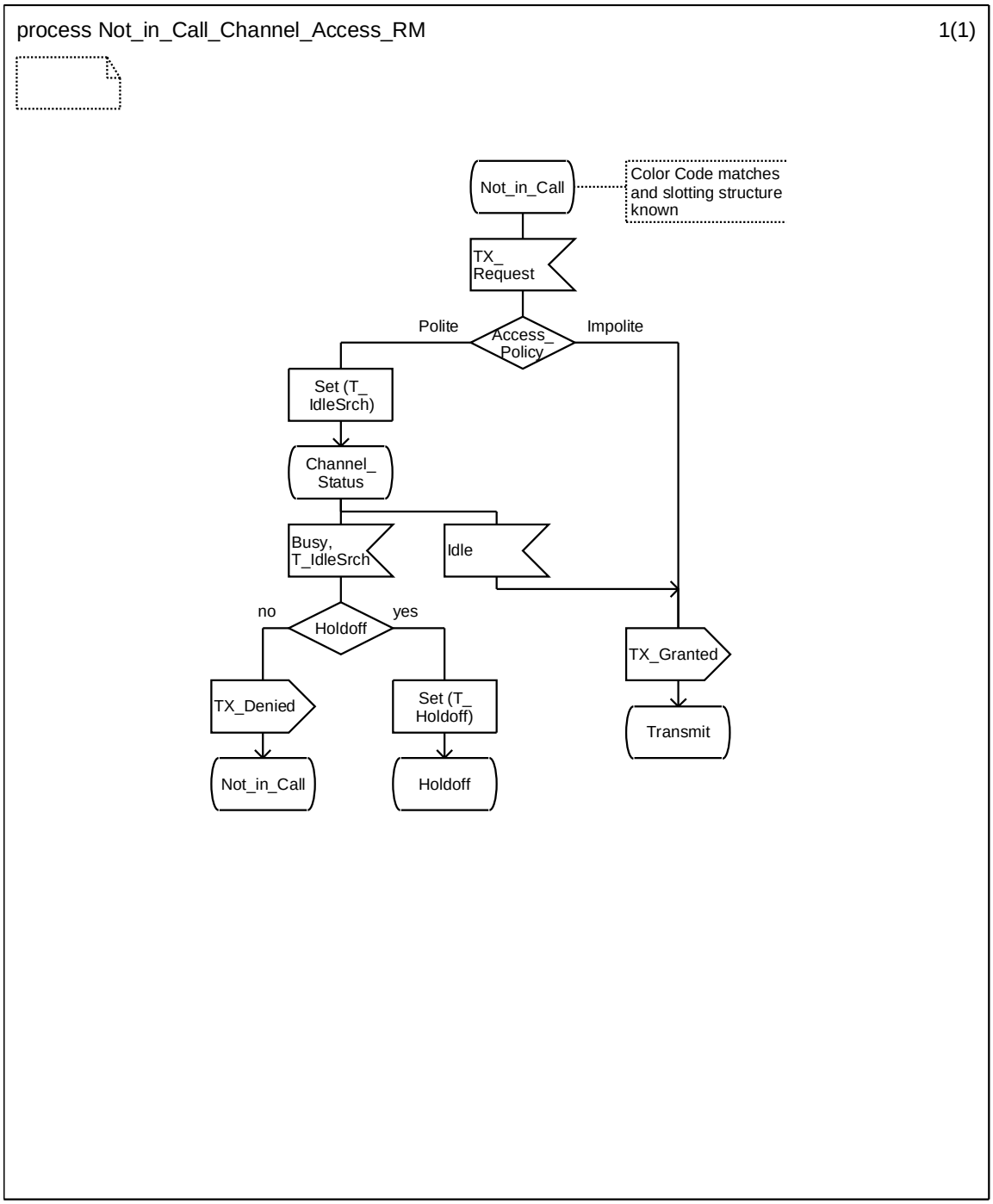


Figure 5.34: Not_in_Call SDL diagram

5.2.2.2.6 MS Others_Call channel access

The MS will grant a transmission from the Others_Call state if the channel access policy is impolite. It will deny or queue the transmission if the channel access policy is polite.

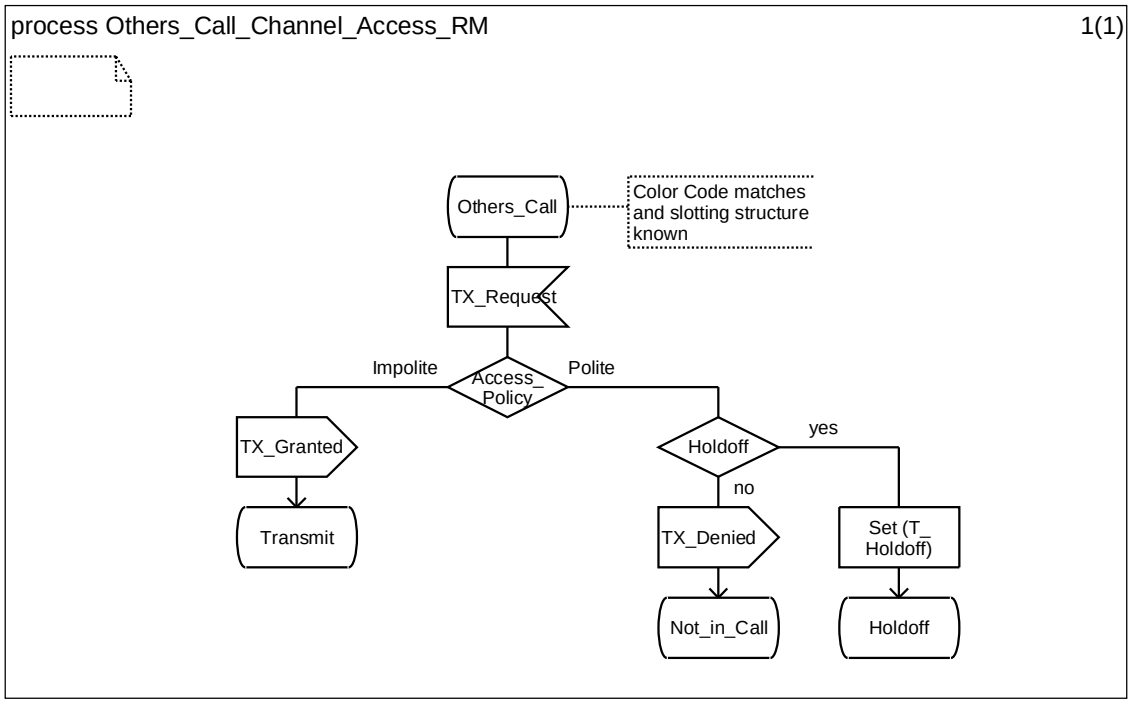


Figure 5.35: Others_Call SDL diagram

5.2.2.2.7 MS My_Call channel access

In this state the MS is party to the call and will use the impolite channel access method for voice calls. This is regardless of the programmed channel access policy programmed into the MS.

5.2.2.2.8 MS In_Session channel access

In this state the MS is party to the call and will use the impolite channel access method for voice calls. This is regardless of the programmed channel access policy programmed into the MS.

5.2.2.3 Non-time critical CSBK ACK/NACK channel access

Figure 5.36 illustrates the MS DLL when the MS receives an individually addressed CSBK that requires a non-time critical response. The response may be either an ACK or a NACK and channel access may be either impolite or polite. The actual channel access rules for features requiring CSBK transmission are defined in ETSI TS 102 361-2 [5]. This may include the addition of counters or timers to limit how long an MS will attempt a CSBK transmission when the channel is busy.

The DLL receives a TX_CSBK primitive from the CCL while in the TX_Idle state. TX_Idle is a general state when the MS is currently not attempting to transmit. When employing polite channel access responses and attempting to transmit the NACK_Rsp, the MS DLL starts the Idle_Search Timer T_IdleSrch and transitions to the Qualify_Idle state. In this state if the channel is idle, the message is transmitted. However, while in this state if the timer expires or the channel is busy a Random_Holdoff timer is started. Upon the expiration of this timer the MS transitions back to the Qualify_Idle state. It is the responsibility of the DLL to attempt to transmit the message.

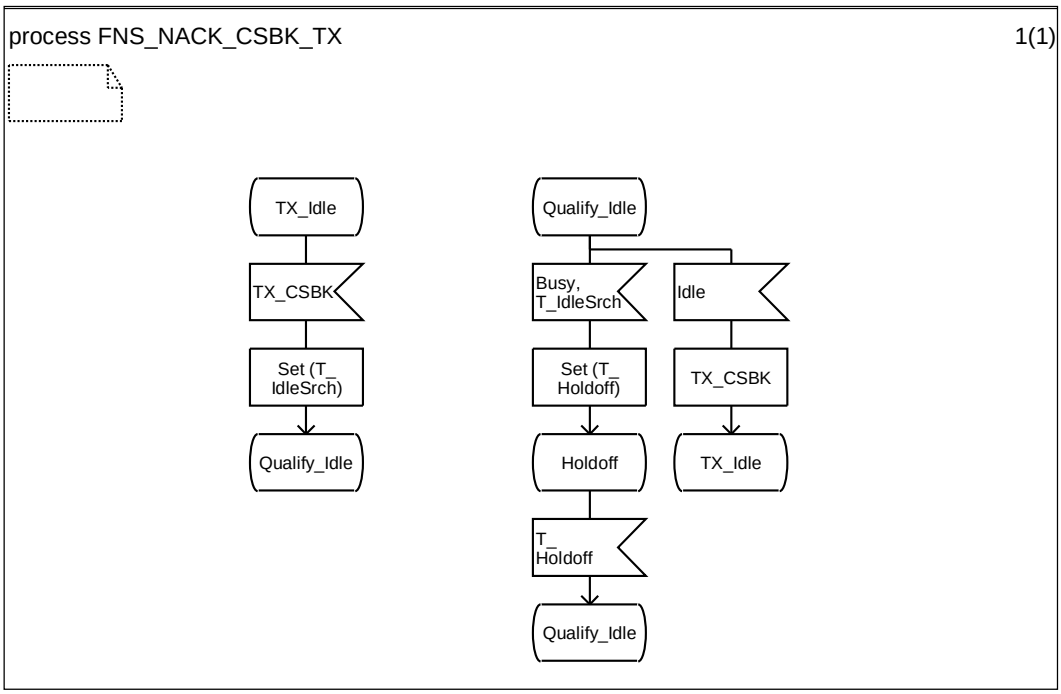


Figure 5.36: FNS channel access SDL diagram

5.2.2.4 TDMA direct mode channel access

5.2.2.4.0 TDMA direct mode channel access - Introduction

TDMA direct mode channel access is designed to use any of the 3 existing ETSI DMR types of channel access settings; ***Impolite, Polite to own Color Code and Polite to All***. An MS operating in TDMA direct mode shall be programmed to operate on Slot 1 or Slot 2. In TDMA direct mode it is possible to initiate channel access from any of the high level MS states as defined in annex G. These high level states include PS_OutOfSync, PS_InSyncUnknownSystem, PS_NotInCall and PS_OthersCall or PS_MyCall. It is also possible to request channel access while in PS_OutOfSyncChMon.

5.2.2.4.1 MS Out_of_Sync channel access

The three access mechanisms from the High Level MS Out_of_Sync state are illustrated in figure 5.37. This is an informative SDL diagram that generically shows transmission request from the Out_of_Sync state. In the Out_of_Sync state the MS has not resided on the channel long enough to immediately know the status of the channel. Therefore it shall attempt to qualify the channel status. Additionally for completeness, figure 5.37 shows how transitions from Out_of_Sync state to either Out_of_Sync_Channel_Monitored or In_Sync_Unknown_System states occur.

A transmission request employing impolite channel access from the High Level MS Out_of_Sync state shall be granted after monitoring the channel for current activity. If neither of the TDMA direct mode time slot synchronization patterns are detected during the search period, then the MS shall transmit with the channel slot timing if known. If the channel slot timing is not known, the MS shall transmit using timing rules defined in [5]. If only the TDMA direct mode synchronization pattern for the non-desired transmission time slot is detected during the search period, then the MS shall synchronize, adjust timing by 30 ms and transmit. If the TDMA direct mode synchronization pattern for the desired transmission time slot is detected during the search period, then the MS shall synchronize to the desired time slot and transmit if the colour code is not the All System Color Code, 0xF. If the channel activity contains the All System Color Code then the MS may deny the transmission request.

A transmission request employing polite to all channel access policy from the High Level Out_of_Sync state shall determine the RF level present on the channel after it fails to detect any TDMA direct mode synchronization pattern. If the measured RF level is less than the programmed RF threshold, then the transmission is granted and the MS shall transmit with the channel slot timing if known. If the channel slot timing is not known, the MS shall transmit using timing rules defined in [5]. If the measured RF level is greater than or equal to the programmed N_RssiLo then the MS shall yield to the current channel activity and deny the transmission or places it in queue. If only the TDMA direct mode synchronization pattern for the non-desired transmission time slot is detected then the MS shall synchronize, adjust timing by 30 ms and measure the RF level in the desired transmission time slot. If the measured RF level is greater than or equal to the programmed N_RssiLo, then the MS shall yield to the current channel activity and deny the transmission or places it in queue. If the measured RF level is less than the programmed RF threshold, then the transmission is granted. If the TDMA direct mode synchronization pattern for the desired transmission time slot is detected, then the MS shall measure the RF level. If the measured RF level is greater than or equal to the programmed N_RssiLo, then the MS shall yield to the current channel activity and deny the transmission or places it in queue. If the measured RF level is less than the programmed RF threshold, then the transmission is granted.

A transmission request employing polite to colour code channel access policy from the High Level Out_of_Sync state shall be granted after it fails to detect any TDMA direct mode synchronization pattern. The MS shall transmit with the channel slot timing if known. If the channel slot timing is not known, the MS shall transmit using timing rules defined in [5]. If only the TDMA direct mode synchronization pattern for the non-desired transmission time slot is detected then the MS shall synchronize, adjust timing by 30 ms and transmit. If the TDMA direct mode synchronization pattern for the desired transmission time slot is detected, then the MS shall attempt to decode the Colour Code. If the Colour Code does not match or is the All System Color Code (0xF), then the MS grants the transmission. If the Colour Code matches or is the All System Color Code, then the transmission is denied or placed in queue and the MS moves to the High Level Not_in_Call state.

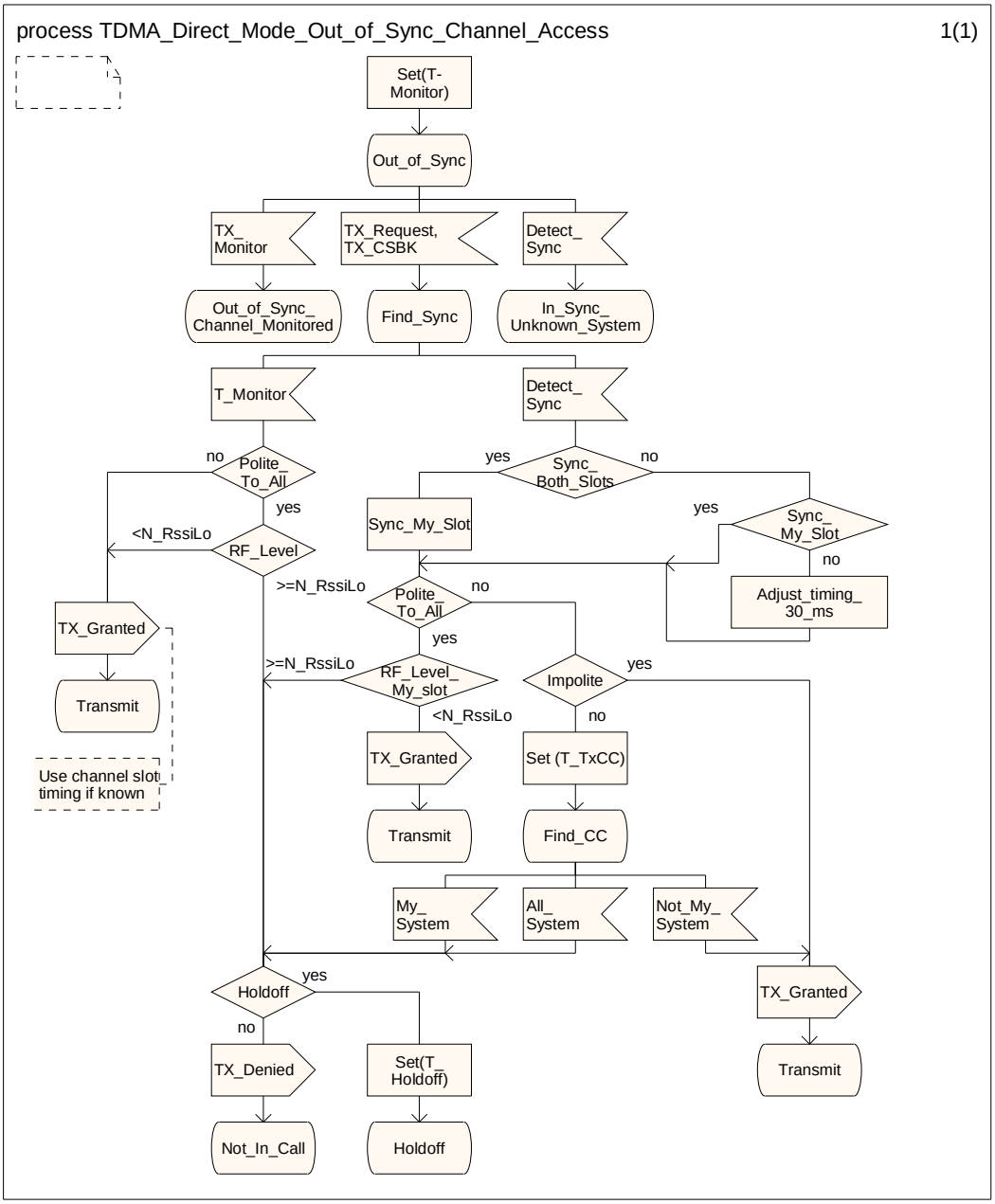


Figure 5.37: Out_of_Sync SDL diagram

5.2.2.4.2 MS Out_of_Sync_Channel_Monitored channel access

The three access mechanisms from the Out_of_Sync_Channel_Monitored state are illustrated in figure 5.38. This informative SDL diagram describes a transmission request when the MS knows the channel is currently idle with respect to DMR activity and also knows the RF level on the channel.

All transmissions from this state shall be granted except when the polite channel access type is polite to all and the RF level exceeds N_RssiLo. In this case the MS shall deny the transmission or placed it in queue.

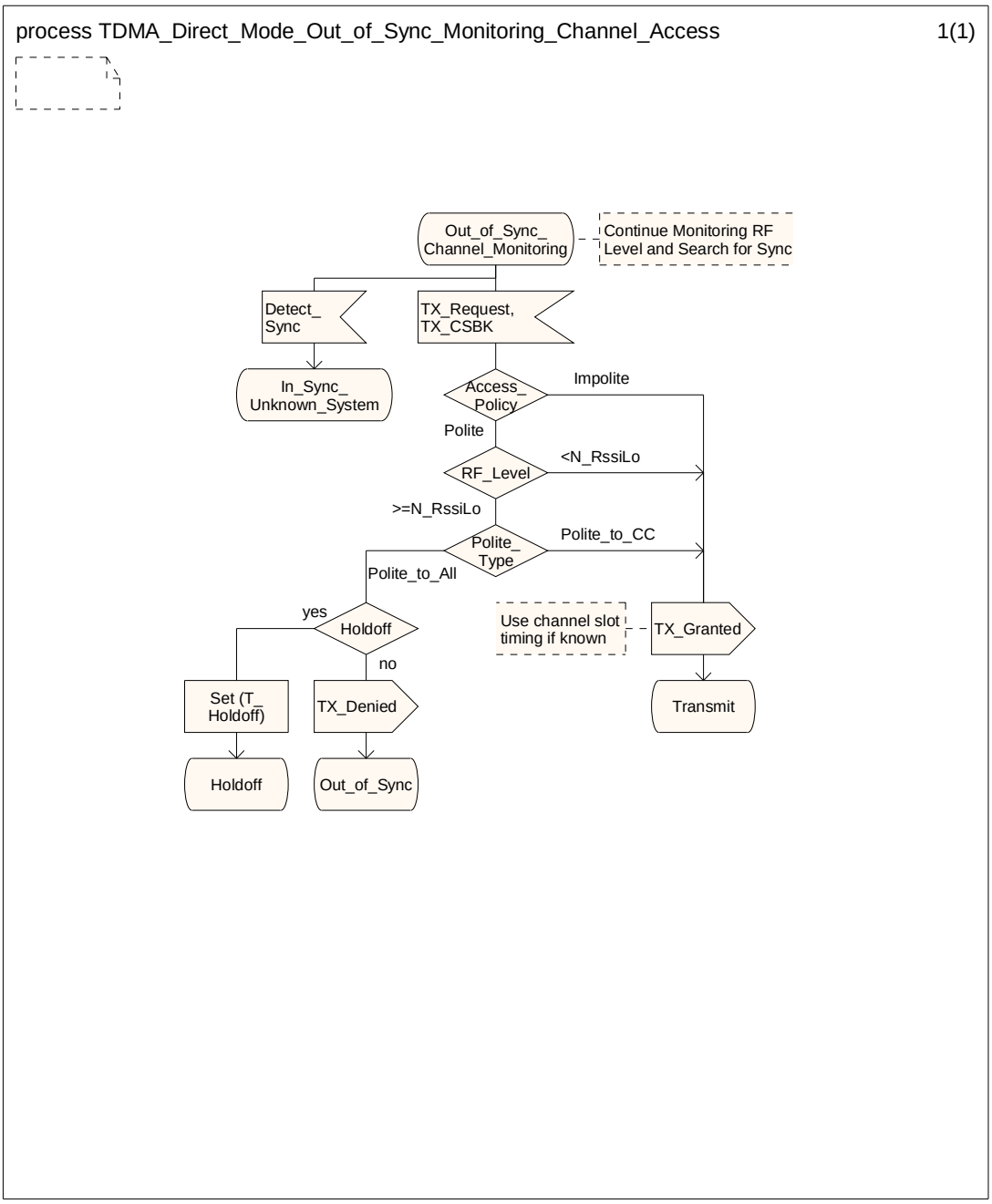


Figure 5.38: Out_of_Sync_Channel_Monitored SDL diagram

5.2.2.4.3 MS In_Sync_Unknown_System channel access

The three access mechanisms from the High Level MS In_Sync_Unknown_System state are illustrated in figure 5.39.

A transmission request employing impolite channel access policy from the High Level MS In_Sync_Unknown_System state is always granted unless the activity utilizes the All System Colour Code. If the activity is the All System Colour Code then the transmission request may be granted.

A transmission request employing a polite channel access type of polite to all from the High Level In_Sync_Unknown_System state shall deny the transmission or place in queue if the desired transmission slot RF level is greater than or equal to N_RssiLo. The MS shall grant the transmission if the desired transmission RF level is less than N_RssiLo.

A transmission request employing a polite channel access type of polite to own Colour Code from the High Level MS In_Sync_Unknown_System shall start the TX_CC_Timer (T_TxCC). Here the MS attempts to determine the Colour Code on the channel. From this point the channel access is the same as from this point when channel access is requested from the High Level Out_of_Sync state.

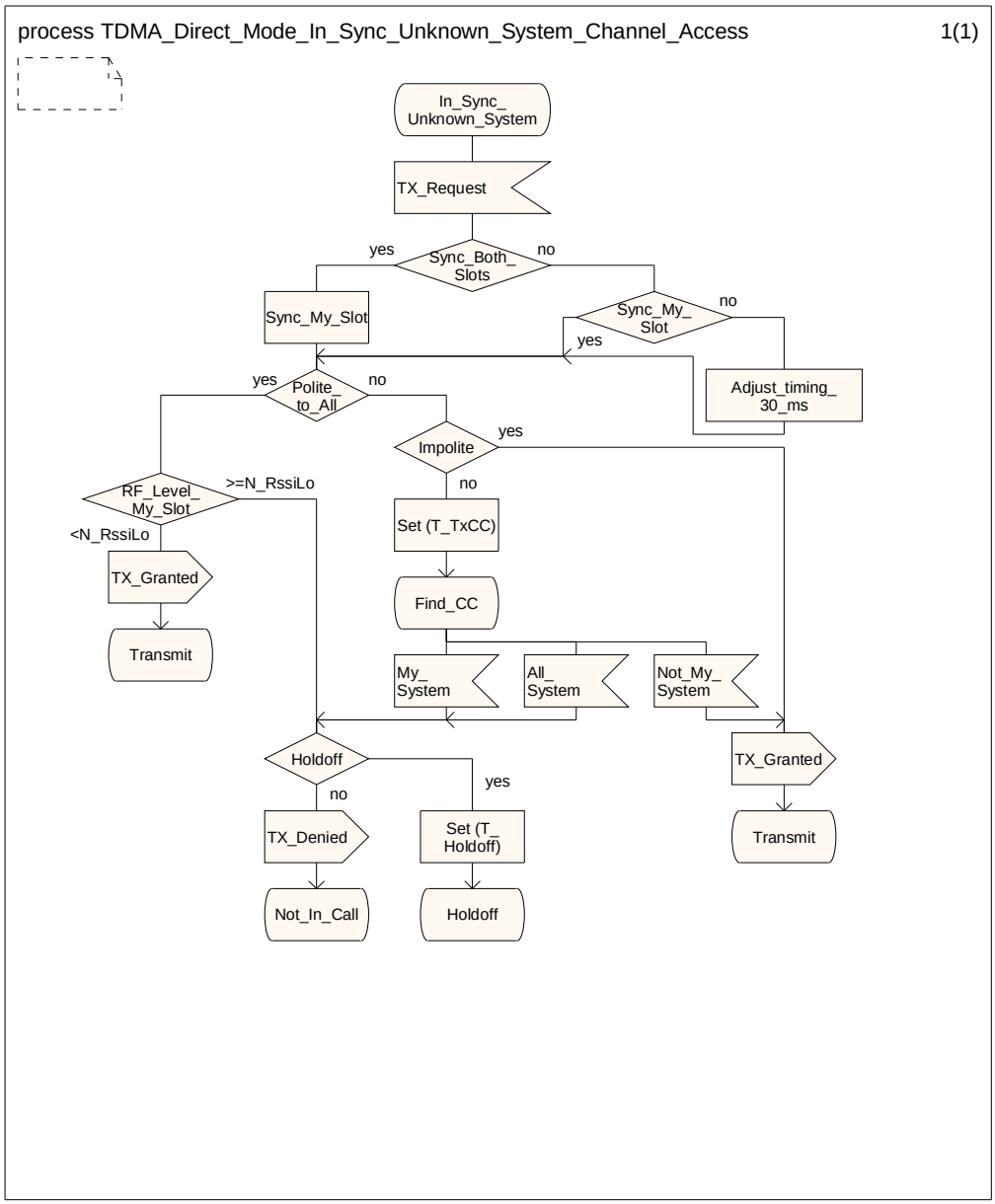


Figure 5.39: In _Sync_Unknown_System SDL diagram

5.2.2.4.4 MS Not_in_Call channel access

A transmission request employing impolite channel access policy from the High Level MS Not_in_Call state is always granted.

A transmission request employing either polite channel access policy type from the High Level Not_in_Call state shall be denied or placed in queue if it is non-time critical. (In order to reach this state the MS has matched the Colour Code.) The MS stays in the Not_in_Call state.

5.2.2.4.5 MS Others_Call channel access

A transmission request employing impolite channel access policy from the High Level MS Others_Call state is always granted.

A transmission request employing either polite channel access policy type from the High Level Others_Call state will be denied or placed in queue if it is non-time critical. (In order to reach this state the MS has matched the Colour Code.) The MS stays in the Others_Call state.

5.2.2.4.6 MS My_Call channel access

In this state the MS is party to the call and uses the impolite channel access method. This is regardless of the programmed channel access policy programmed into the MS. In this case the transmission shall use the channel slot timing of the call to which it is a party.

5.2.2.4.7 Immediate response channel access

In TDMA direct mode there are instances where an MS needs to respond quickly (~90 ms) after reception of an individually addressed message. Examples are Confirmed Data Responses (clause 5.4.2 of ETSI TS 102 361-3 [12]) and OACSU Individual call (clause 5.2.2 of ETSI TS 102 361-2 [5]) ACK/NACK CSBKs. In these cases the target MS shall transmit the response with the channel slot timing of the received message. A CT_CSBK_Terminator is transmitted by the source MS to reserve the channel (clause 6.2.2.3.3 of ETSI TS 102 361-2 [5]) and preserve the channel slot timing.

6 Layer 2 burst format

6.0 Layer 2 burst format - Introduction

The following clauses define the burst formats and channels for DMR. This includes voice bursts, general data bursts, and the Common Announcement Channel. The bursts contain user data and/or signalling encapsulated in Protocol Data Units (PDUs), with its associated bits for error detection and/or correction. The PDUs and its information elements that are carried by these bursts are defined in detail in clause 9. The burst definition diagrams use the legends shown in figure 6.1. The exact bit position within a burst is defined in annex E.

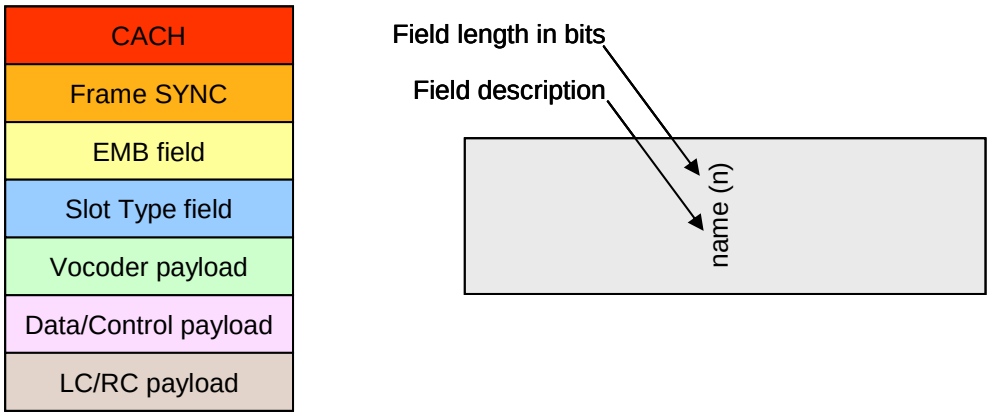


Figure 6.1: Colour legends

6.1 Vocoder socket

The vocoder bits are carried in a voice burst over the air as shown in figure 6.2. Each voice burst provides a "vocoder socket" for 2 × 108 bits vocoder payload (VS) to carry 60 ms of compressed speech. The vocoder bits are labelled VS(0) - VS(215) and are placed in the burst as shown in figure 6.2.

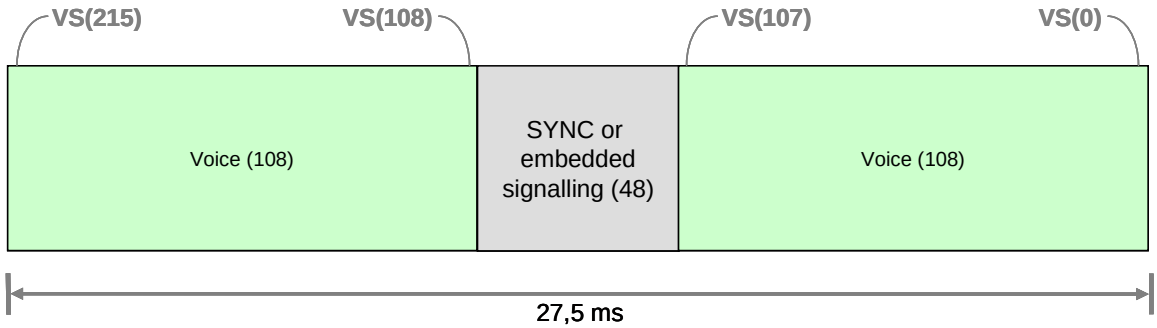


Figure 6.2: Generic voice burst

Usually more than one vocoder frame is transmitted in the same burst. Each Voice burst is capable of transferring M vocoder frames called VF(1), VF(2), … VF(M) where the vocoder outputs VF(1) before VF(2) and so on, giving them in this order to the transmission path. If this is the case the order of the vocoder frames contained in the same burst shall be such that the MSB of VF(1) is transmitted as VS(215) and the LSB of VF(M) is transmitted as VS(0). All the bits of a given voice frame should be placed contiguously in the burst.

In addition to vocoder bits, these voice bursts carry either embedded signalling (EMB field + embedded signalling) or frame synchronization (SYNC) in the centre of the burst. This same format is used for both inbound and outbound bursts.

Figure 6.3 illustrates a voice burst containing frame synchronization. The SYNC pattern is described in clause 9.1.1.

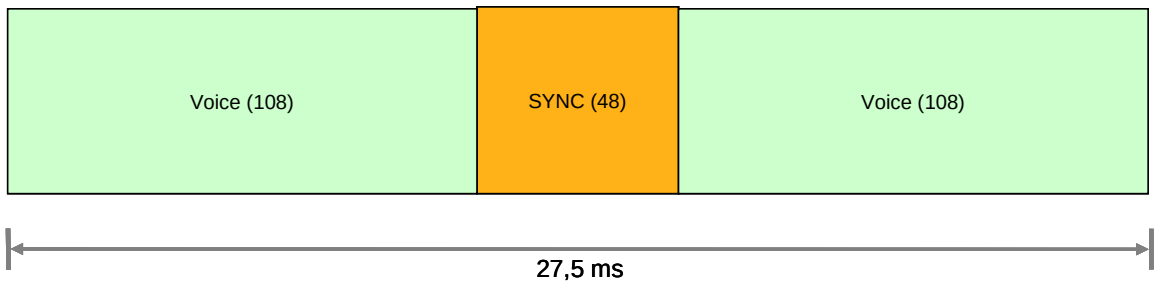


Figure 6.3: Voice burst with SYNC

Figure 6.4 illustrates a voice burst containing embedded signalling and shows the parameters of the EMB field.

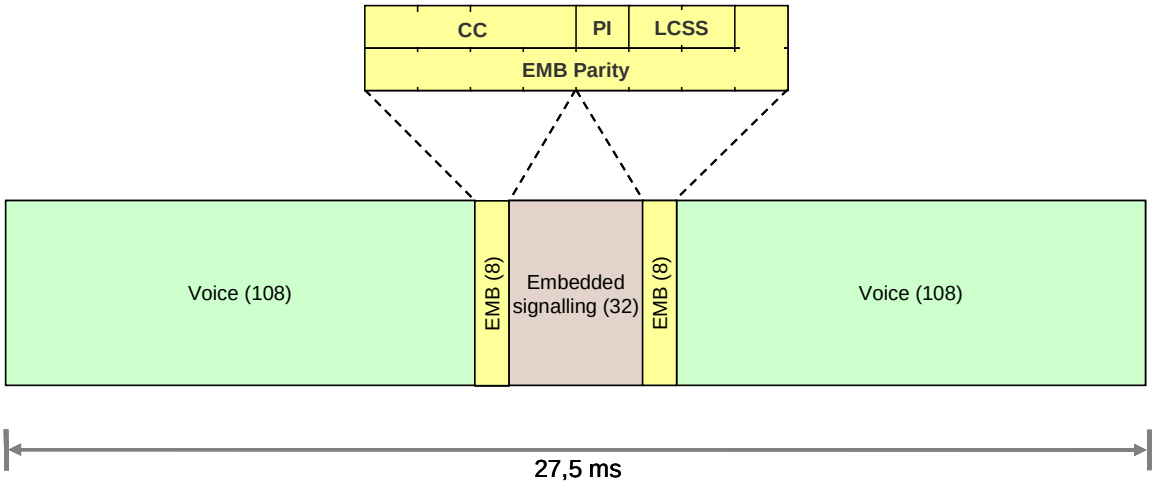


Figure 6.4: Voice burst with embedded signalling

The embedded signalling is either Link Control (LC), Reverse Channel (RC) information, information related to Privacy (not defined in the present document) or Null embedded message (see clause D.1).

6.2 Data and control

A single burst format shall be used for data and control, both inbound and outbound, as shown in figure 6.5. Also shown are the symbol numbers, counting Left (L) and Right I from the burst centre, of the information element boundaries.

Either a data SYNC or embedded signalling information shall be provided in the centre of every control burst in a manner similar to the voice bursts. Every data and control burst contains a 20-bit Slot Type PDU (SLOT) that defines the meaning of the 196 information bits. The purpose of the Data Type information element of the SLOT PDU shall be as defined in table 6.1 which shows also the used payload FEC. The detailed coding is described in clause 9.3.6. The SYNC pattern is described in clause 9.1.1.

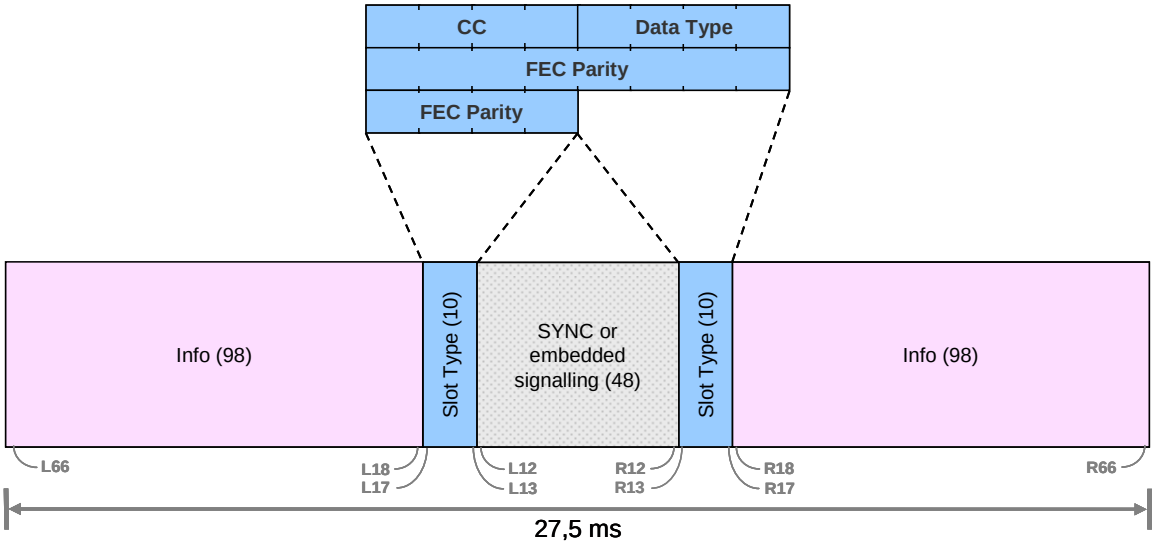


Figure 6.5: General data burst

Table 6.1: Data Type information element definitions

Data Type	Purpose	Payload FEC
PI Header, see note	Privacy Indicator information in a standalone burst	BPTC(196,96)
Voice LC Header	Indicates the beginning of voice transmission, carries addressing information	BPTC(196,96)
Terminator with LC	Indicates the end of transmission, carries LC information	BPTC(196,96)
CSBK	Carries a control block	BPTC(196,96)
MBC Header,	Header for multi-block control	BPTC(196,96)
MBC Continuation	Follow-on blocks for multi-block control	BPTC(196,96)
Data Header	Carries addressing and numbering of packet data blocks	BPTC(196,96)
Rate ½ Data Continuation	Payload for rate ½ packet data	BPTC(196,96)
Rate ¾ Data Continuation	Payload for rate ¾ packet data	Rate ¾ Trellis
Idle	Fills channel when no info to transmit	BPTC(196,96)
NOTE: This information element is not defined in the present document and is reserved for future use.		

6.3 Common Announcement Channel burst

The CACH exists on the outbound channel only. This field provides framing and access information for the bursts as well as low-speed data. This channel is not tied to channel 1 or 2 but is common between them, as shown in figure 6.6.

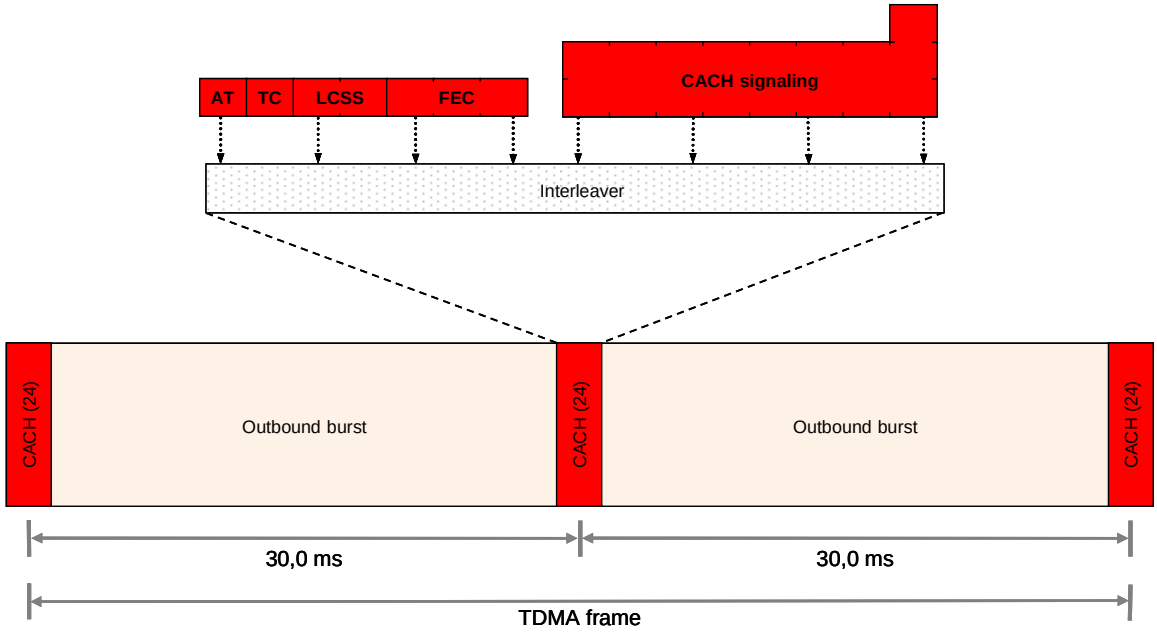


Figure 6.6: CACH burst

Of the 24 bits present in each CACH burst, 4 information and 3 parity bits are dedicated to framing and status. These bits, termed the TDMA Access Channel Type (TACT) bits, are protected by a Hamming (7,4) FEC code. The remaining 17 bits of each CACH burst carry signalling. No FEC is provided by the CACH for this signalling. Instead, any FEC and CRC is part of the payload, see clause B.2.3.

Since this is a common channel, not tied to either the channel 1 or 2, CACH bursts occur every 30 ms. This results in an overall payload bit rate of (17 bits/burst) / (30 ms/burst) = 566,67 bits/s.

Where DMR activity is present on the outbound channel, then the AT bit in each CACH shall indicate to MSs whether the next slot on the inbound channel whose TDMA channel number is indicated by the TC bit (see figure 5.23 for details of the timing relationship between the CACH and inbound/outbound slots) is "Idle" or "Busy".

Typically a BS shall set the AT to "Busy" while DMR activity is present on the inbound channel. Additionally, BSs may also set the AT bit to "Busy" during the call hang time periods for voice calls and whenever activity (e.g. an acknowledgement) is anticipated on the inbound channel.

NOTE: LCSS indicates that this burst contains the beginning, end, or continuation of an LC or CSBK signalling. Due to the small number of bits available, there is no single fragment LC signalling defined.

The number of CACH fields that are combined for a PDU shall not change during a BS outbound transmission. This will improve MS decode reliability.

6.4 Reverse Channel

6.4.1 Standalone inbound Reverse Channel burst

A standalone inbound RC burst allows a MS to send RC signalling on an inbound channel to a BS and or directly to another MS in direct mode. This burst combines both a 48-bit RC SYNC word and a 48-bit embedded signalling field into a single burst as shown in figure 6.7. The use of previously defined fields allows the reuse of existing FEC codes and processing software for this burst type.

Combining the SYNC word and signalling in the same burst allows the MS to send the information in a single 30 ms window for low latency. Limiting the size to 96 bits allows a MS to transition from receiving traffic on one TDMA channel to transmitting RC signalling on the other TDMA channel and back within a 30 ms window.

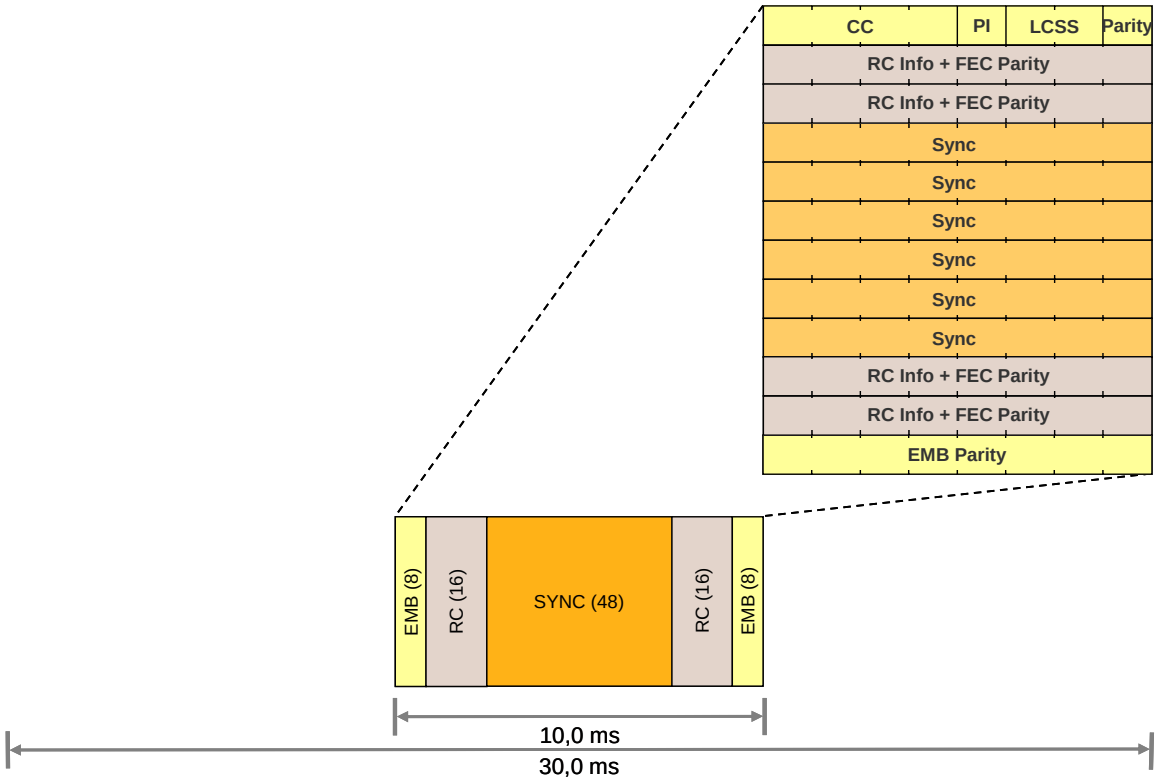


Figure 6.7: Standalone inbound Reverse Channel (RC) burst

The SYNC pattern is placed at the centre of the burst, as it is in all other bursts, so that a receiver can detect it using its normal SYNC detection mechanisms (see note). The signalling information is evenly distributed on either side of the SYNC for symmetry, providing the same transition time for a MS switching from RX to TX and from TX back to RX.

The 11 bits of RC signalling is carried in the 32-bit field, labelled RC info + FEC Parity in figure 6.7. The LCSS field shall be set to indicate a single fragment LC packet. All other fields shall be set according to the current system configuration and mode of operation.

NOTE: Processing this RC burst is optional. The BS ignores the RC burst if it does not support RC signalling.

6.4.2 Outbound reverse channel (RC) burst

An embedded outbound RC burst allows the BS to send RC signalling on the other logical channel of the intended target MS within a traffic channel. This burst places the RC signalling in a single embedded 48-bit EMB/LC field as shown in figure 6.8.

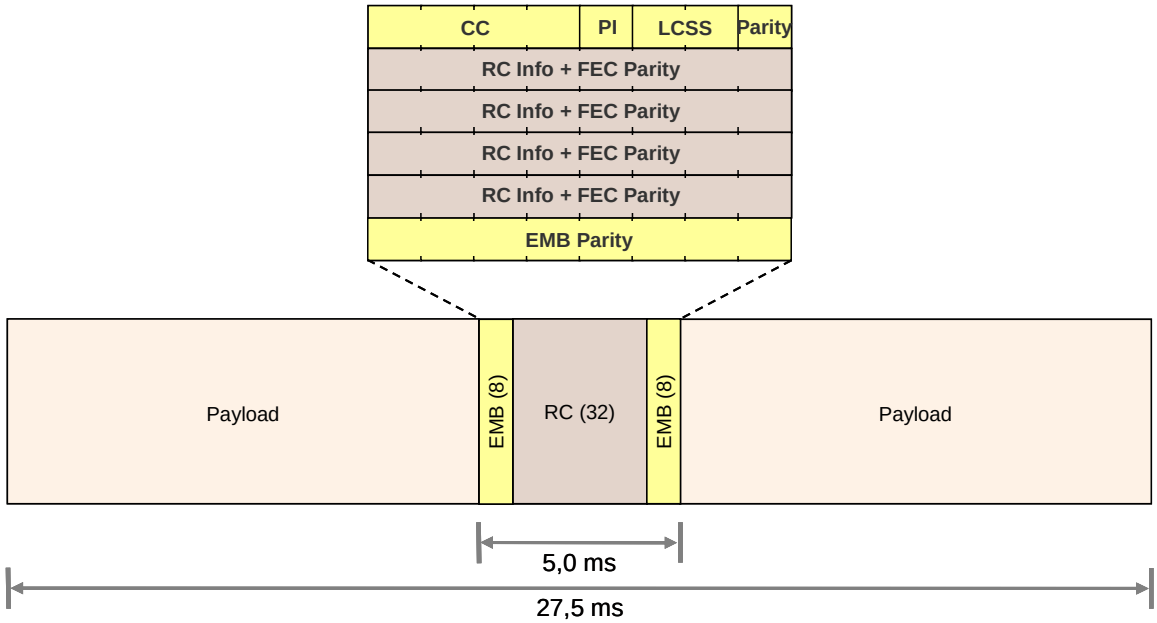


Figure 6.8: Outbound Reverse Channel (RC) burst

The RC signalling is carried in an 11-bit field RC Info and is FEC encoded (Single Burst RC BPTC) and interleaved as described in clause B.2.2.2. The RC signalling is composed of 4-bit field RC payload and an7-bit CRC as described in clause B.3.13. Before the Single Burst RC BPTC encoder, the appropriate CRC Mask as defined in clause B.3.12 of the present document shall be applied to the 7 bit CRC. The LCSS field shall be set to indicate a single fragment LC packet. The PI field shall be set to indicate a packet containing RC information. All other fields shall be set according to the current system configuration and mode of operation.

NOTE: The payload, as seen in figure 6.8, may be either vocoder bits for voice bursts or data plus slot type for data bursts.

7 DMR signalling

7.1 Link Control message structure

7.1.0 Link Control message structure - Introduction

For Link Control signalling a Full LC message and a Short LC message is defined.

The Full Link Control message contains a 72-bit information field and is carried by:

- voice and data (embedded);
- headers;
- terminators.

The general structure of the Full Link Control message is shown in figure 7.1.

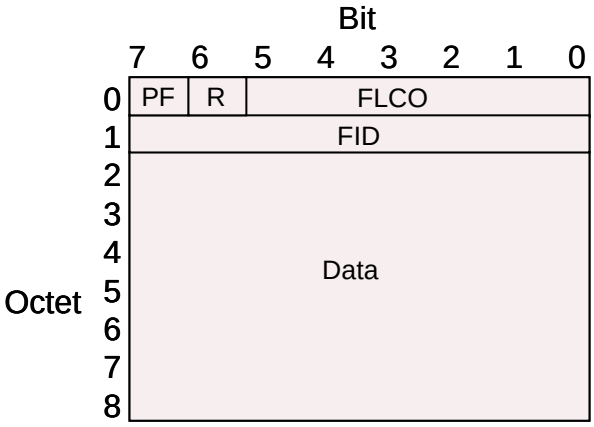


Figure 7.1: Full LC message structure

The Full LC contains 7 octets of data (see note 1) associated with the Full LC Opcode (FLCO) and the Feature ID (FID) combination.

NOTE 1: The DATA information element contains feature specific information (e.g. Source ID and Destination ID) and is defined in ETSI TS 102 361-2 [5].

The Short Link Control message contains a 28-bit information field and is carried by the CACH. The general structure of the Short Link Control message is shown in figure 7.2.

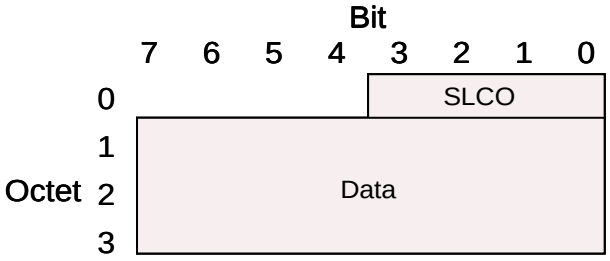


Figure 7.2: Short LC message structure

The Short LC contains 3 octets of data (see note 2) associated with the Short LC Opcode (SLCO).

NOTE 2: The DATA information element contains feature specific information and is defined in ETSI TS 102 361-2 [5].

7.1.1 Voice LC header

When sent, a header burst shall be sent at the start of a voice transmission, using the general data format, to indicate the beginning of a voice transmission (see clause 5.1.2.2). The LC header contains a Full Link Control Header PDU, the general structure of which is described in clause 7.1.

Figure 7.3 illustrates how the 72-bit LC field, along with a 24-bit CRC, is carried in a single general data burst.

Before the BPTC(196,96) encoder, the appropriate Data Type CRC Mask as defined in clause B.3.12 of the present document shall be applied to the 24 bit CRC. The Data Type field of the Slot Type field shall be set to "Voice LC Header".

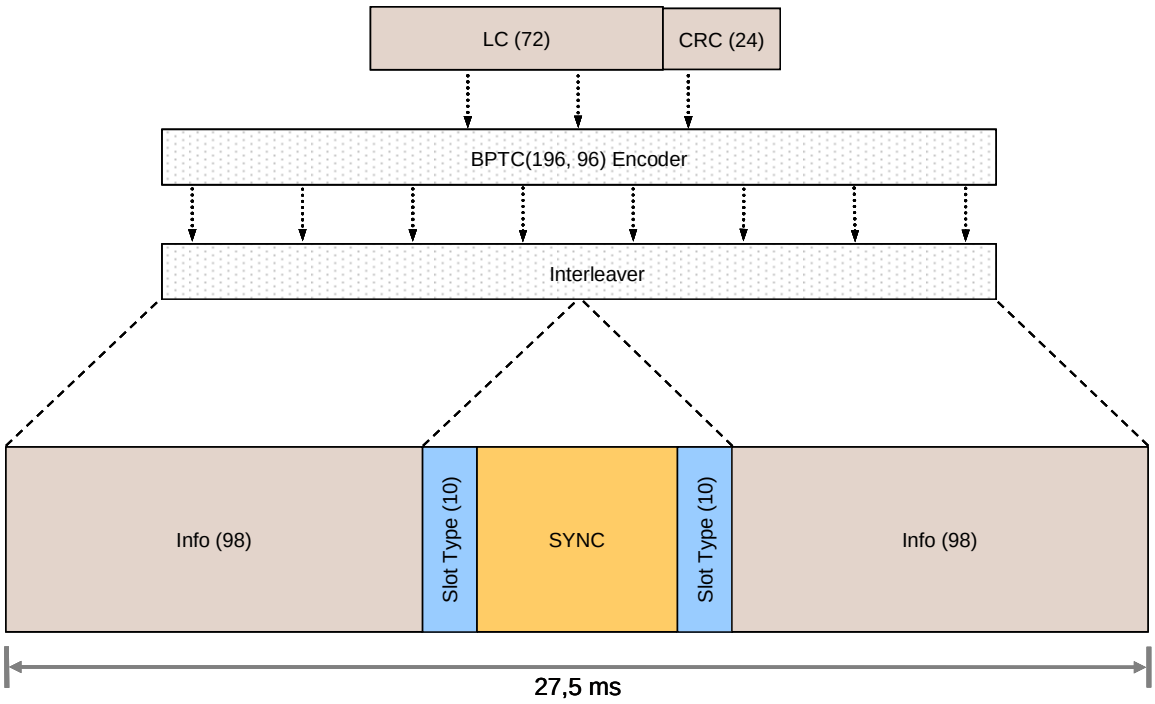


Figure 7.3: LC Voice header format

7.1.2 Terminator with LC

Voice call speech items may be terminated by transmitting a burst containing a data SYNC immediately after the last voice burst.

The 72 bits of LC information are protected using a 24-bit CRC and a BPTC FEC as shown in figure 7.4.

Before the BPTC(196,96) encoder, the appropriate Data Type CRC Mask as defined in clause B.3.12 of the present document shall be applied to the 24 bit CRC. The Data Type field of the Slot Type field shall be set to "Terminator with LC".

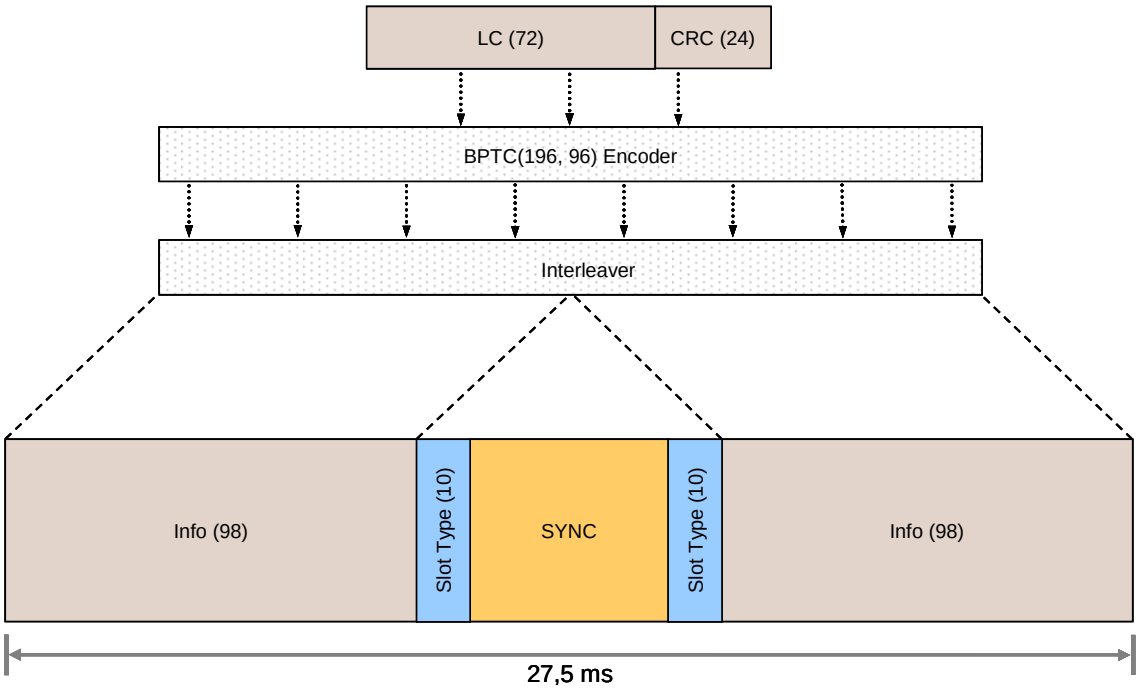


Figure 7.4: Terminator with LC

7.1.3 Embedded signalling

7.1.3.0 Embedded signalling - Introduction

In order to facilitate late entry, LC messages shall be carried in the embedded field of the voice bursts. A 72-bit LC message, after FEC encoding and fragmenting, fits into the embedded field of four bursts as described in clause B.2.1. This means that a 6-burst voice superframe can allocate one burst for SYNC, four bursts for LC, and one burst for the RC (as shown in figure 7.5) or Null embedded message (as shown in figure 7.6).

All four bursts of one LC message shall be carried within a single voice superframe. The LC starts on the first non-SYNC (burst B) of a superframe.

The beginning, continuation, and end of a complete LC message are framed using the LCSS bits of the EMB field as described in clause 6.1. Non-LC embedded signalling types are indicated by setting the LCSS bits to indicate that this burst contains a "Single Fragment LC Packet".

NOTE: The interpretation of these non-LC bursts is dependent on call type and context.

7.1.3.1 Outbound channel

In order to support RC features in the outbound channel, a single burst from each outbound voice superframe shall be dedicated for a RC signalling opportunity, as shown in figure 7.5.

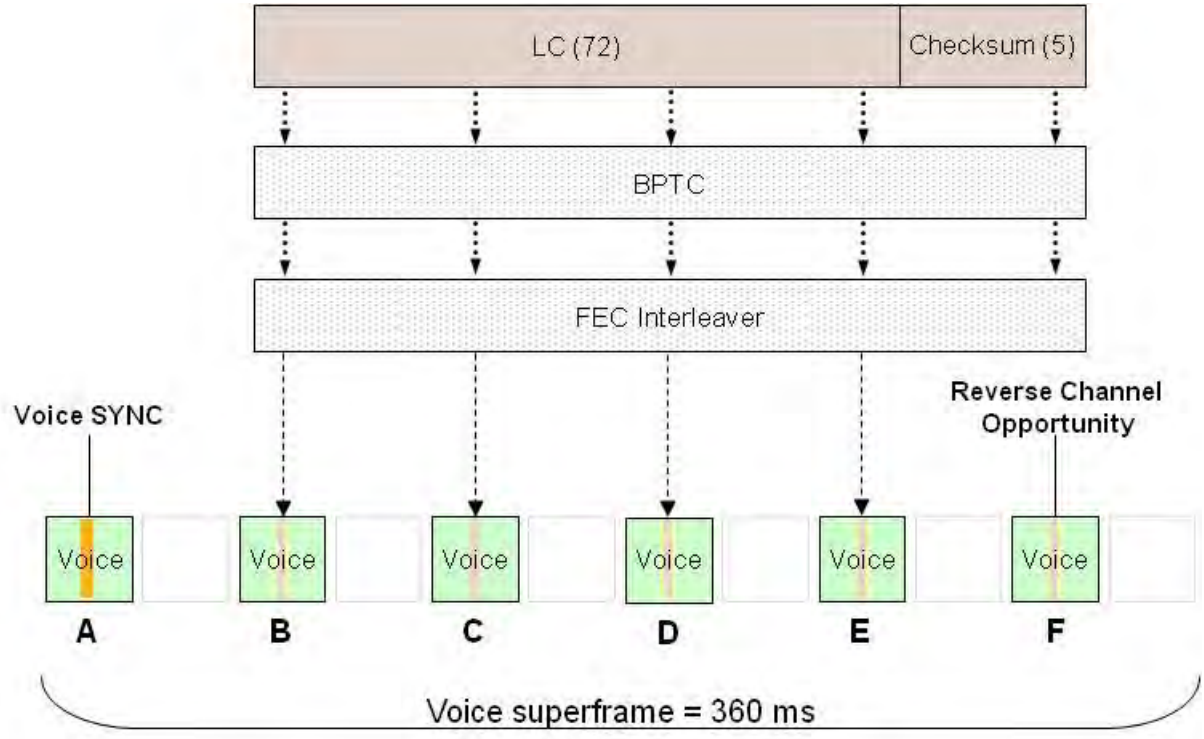


Figure 7.5: Outbound voice superframe example

Burst A always contains a voice SYNC pattern and burst F carries either RC signalling as required as described in clause 5.1.5.1, or repeated inbound information related to Privacy (not defined in the present document) or null embedded message (see clause D.1).

The four remaining voice bursts, B to E, in the voice superframe carry embedded signalling messages. An example outbound voice superframe is shown in figure 7.5, where the F burst is the RC signalling opportunity.

7.1.3.2 Inbound channel

The inbound voice superframe shall not contain a RC, therefore in order to maintain consistent timing between the inbound and outbound LC messages, burst F of an inbound voice superframe shall always be filled with Null embedded message, thereby ensuring that a single LC message is sent in every voice superframe. This is illustrated in figure 7.6.

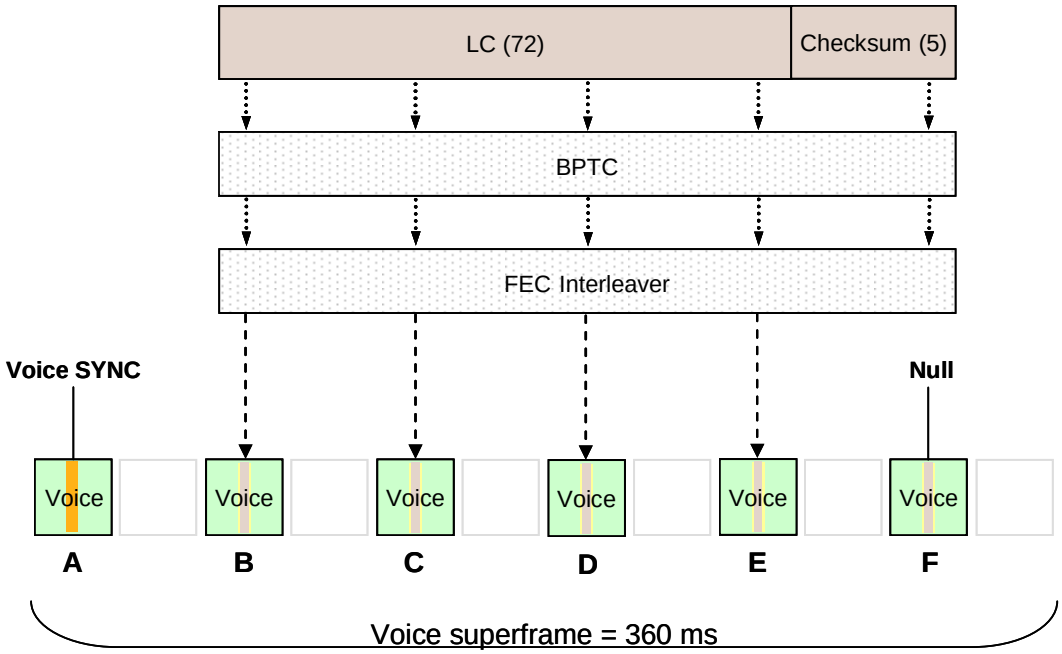


Figure 7.6: Inbound voice superframe

7.1.4 Short Link Control in CACH

A Short LC message has been specifically defined to be carried by the CACH as shown in figure 7.7. The LC PDU has a length of 36 bits and is protected using a block product turbo code as described in clause B.2.3.

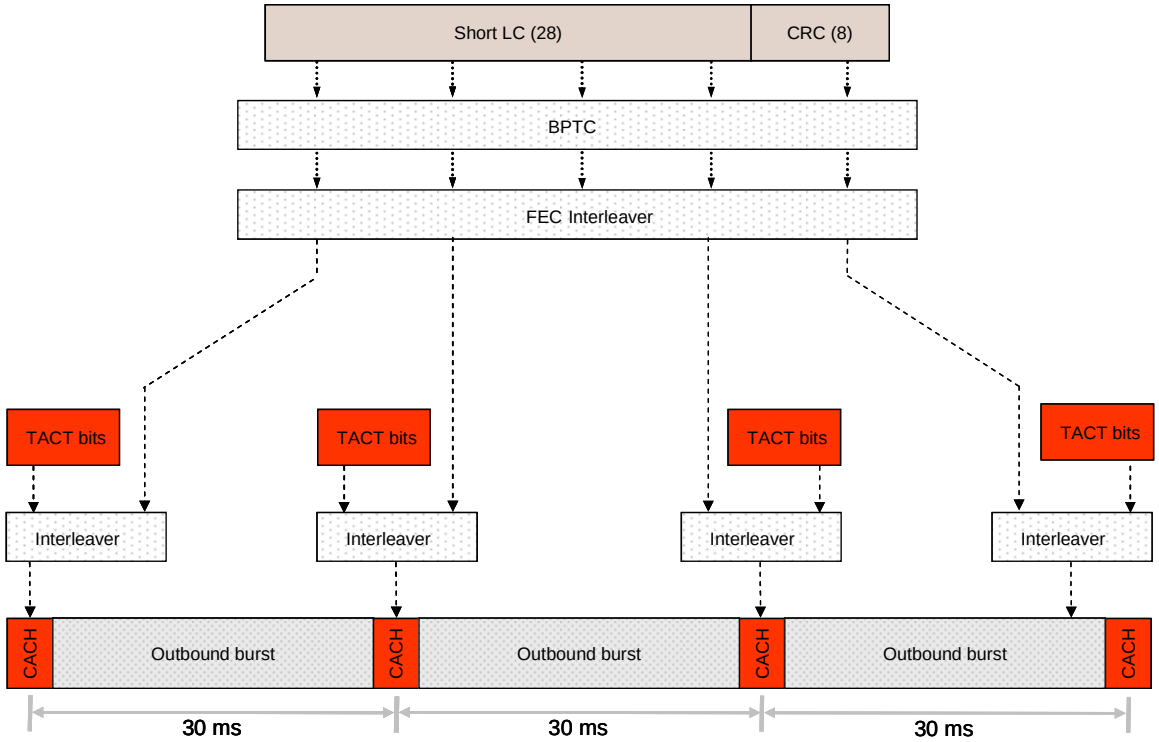


Figure 7.7: Short LC in CACH

The resulting FEC matrix is interleaved over multiple CACH bursts for resistance to errors. Each LC fragment is further interleaved with the CACH TACT bits as it is placed into the CACH field. Since the entire payload can be delivered in 4 CACH bursts, one message can be sent every 4 × 30 ms = 120 ms.

7.2 Control Signalling BlocK (CSBK) message structure

7.2.0 Control Signaling BlocK (CSBK) message structure - Introduction

The CSBK message contains a 96-bit information field.

The general structure of the CSBK message is shown in figure 7.8.

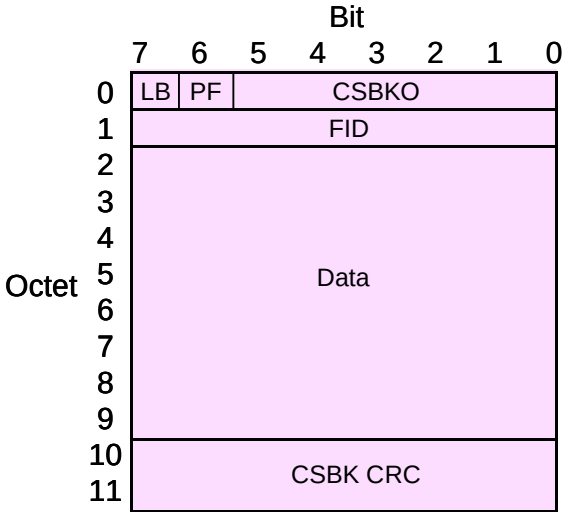


Figure 7.8: CSBK message structure

The CSBK contains 8 octets of data (see note 1) associated with the CSBK Opcode (CSBKO) and the Feature ID (FID) combination. The LB information element shall be set to 1_2.

NOTE 1: The DATA information element contains feature specific information (e.g. Source ID and Destination ID) and is defined in ETSI TS 102 361-2 [5].

NOTE 2: The message structure of a Multiple Block Control (MBC) is defined in clause 7.4.

7.2.1 Control Signalling BlocK (CSBK)

The 96 bit CSBK (80 bits of signalling + 16 bits of CRC) shall be protected by a BPTC(196,96) FEC, as described in clause B.1.1.

Before the BPTC(196,96) encoder, the appropriate Data Type CRC Mask as defined in clause B.3.12 shall be applied to the 16 bit CRC. The information bits can be carried in a single data burst as shown in figure 7.9. The Data Type field of the Slot Type field shall be set to "CSBK".

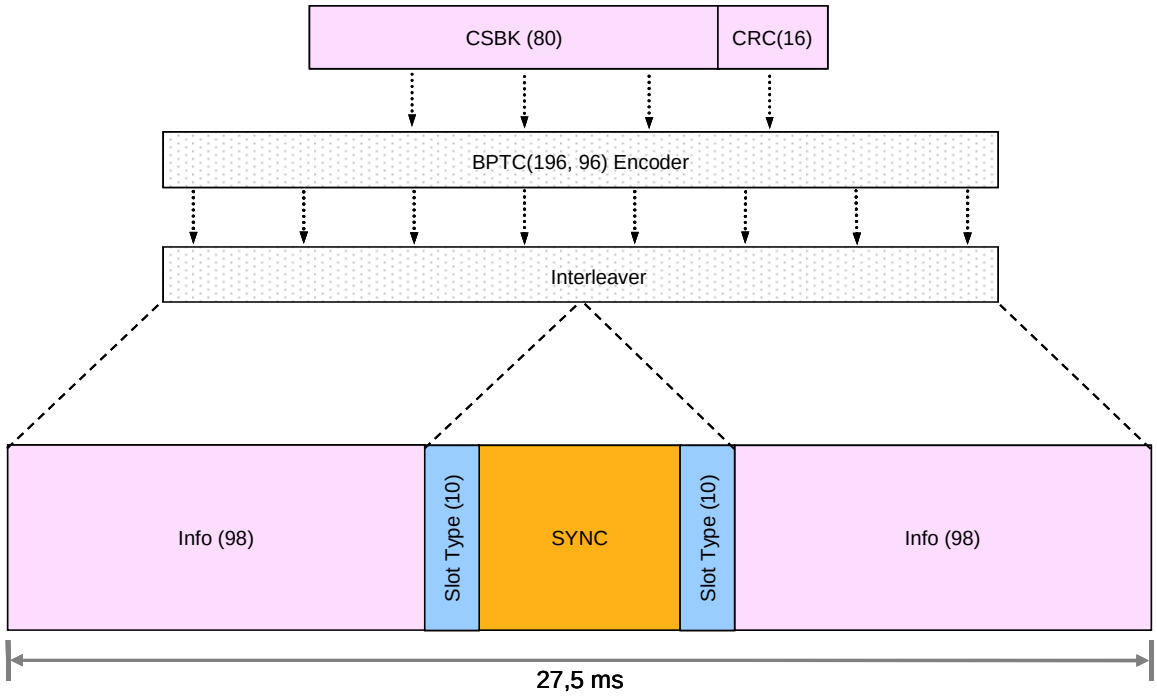


Figure 7.9: CSBK format

7.3 Idle message

Idle messages are transmitted by the BS when it has no other valid signalling or traffic to send. The Data Type field of the Slot Type field shall be set to "Idle". The info fields of Idle messages will be filled with predetermined Pseudo-Random Fill Bits (PR FILL).

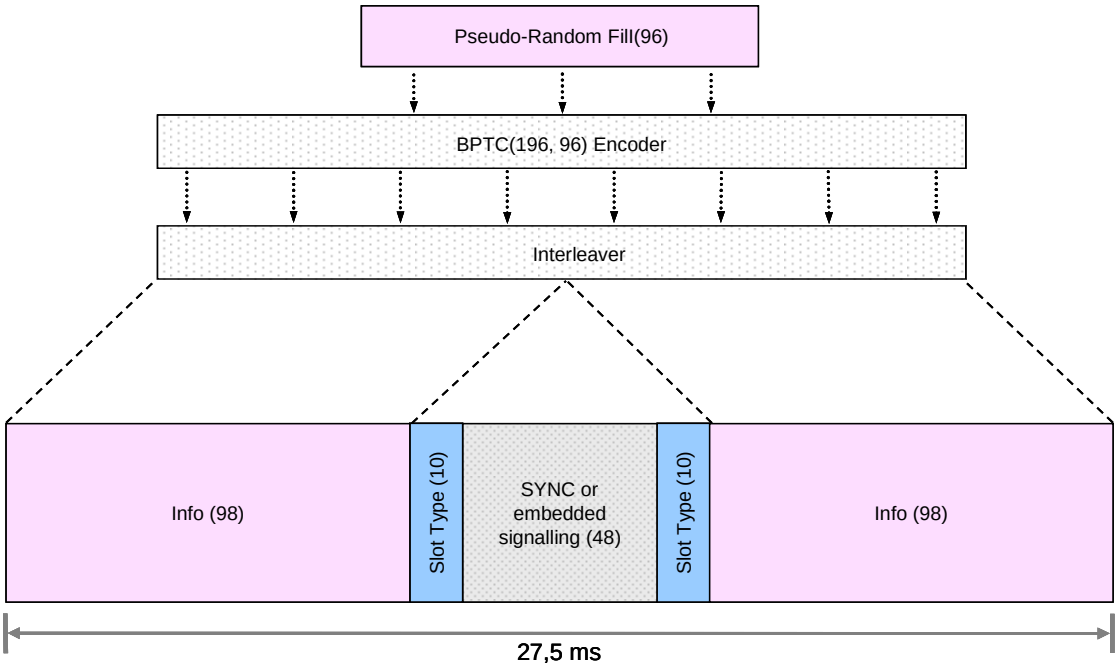


Figure 7.10: Idle message format

These bits are encoded using BPTC(196,96) FEC and interleaver used for normal data and control as shown in figure 7.10. These bits are included only to enable continuous transmission by the BS. They are not intended to be read or processed by the MSs.

7.4 Multi Block Control (MBC) message structure

7.4.0 Multi Block Control (MBC) message structure - Introduction

The MBC message is used when a CSBK cannot carry all of the required control information. The basic format is built upon the CSBK message structure. The MBC message shall consist of a MBC header, between 0 and 2 MBC intermediate blocks and a MBC last block. The general structure of the three different MBC message blocks are shown in figures 7.11 to 7.13.

NOTE 1: MBCs are transmitted contiguously on a slot.

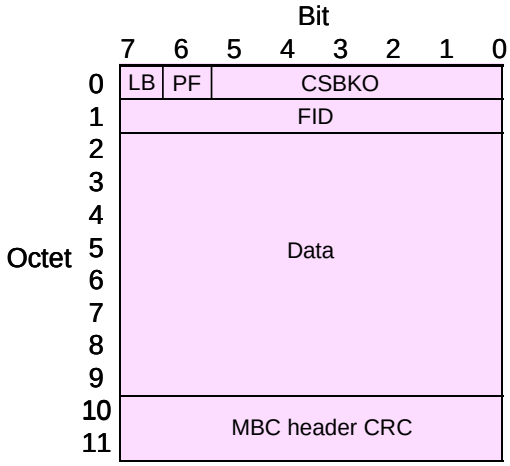


Figure 7.11: MBC header message structure

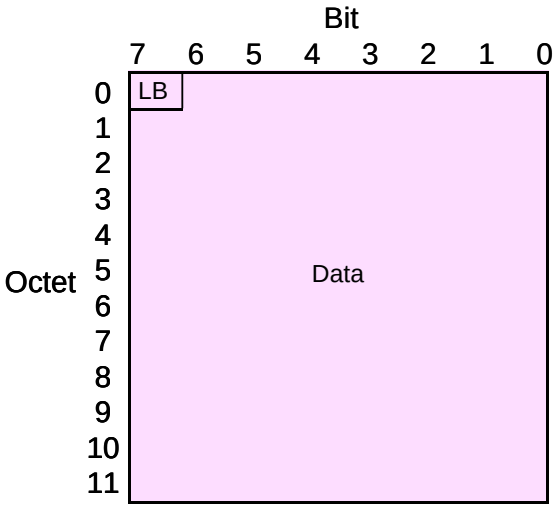


Figure 7.12: MBC intermediate block message structure

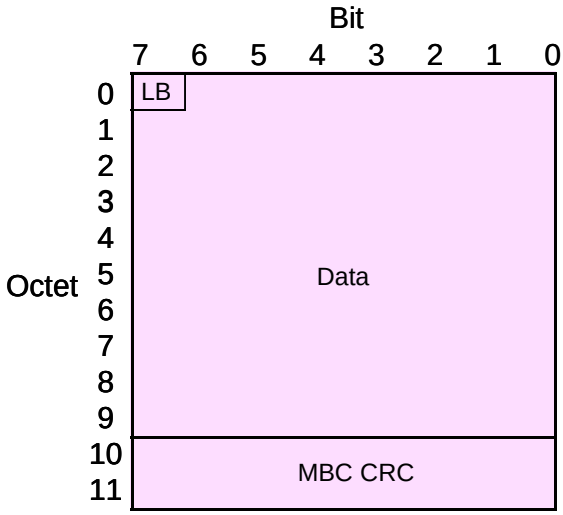


Figure 7.13: MBC last block message structure

The MBC contains data (see note 1) that is associated with the CSBK Opcode (CSBKO) and the Feature ID (FID) combination.

NOTE 2: The DATA information element contains feature specific information and is defined in ETSI TS 102 361-4 [11]. The header block contains 64 bits, an intermediate block contains 95 bits and the last block contains 79 bits.

NOTE 3: A MBC carries up to 333 bits of data when the header is followed by 3 blocks.

The 16 bit CRC in the header shall include the data carried by the header. The 16 bit CRC in the last block shall be performed on all MBC blocks except the header block.

7.4.1 Multi Block Control (MBC)

The MBC header, intermediate and last blocks shall be protected by a BPTC(196,96) FEC, as described in annex B of the present document.

Before the BPTC(196,96) encoder for the MBC header and the MBC last block, the appropriate Data Type CRC Mask as defined in clause B.3.12 of the present document shall be applied to the 16 bit CRC. The information bits are carried in the header, intermediate blocks if necessary and the last block as shown in figures 7.14, 7.15 and 7.16. The Data Type field of the Slot Type field shall be set to "MBC Header" for the header and "MBC Continuation" for the intermediate and last blocks.

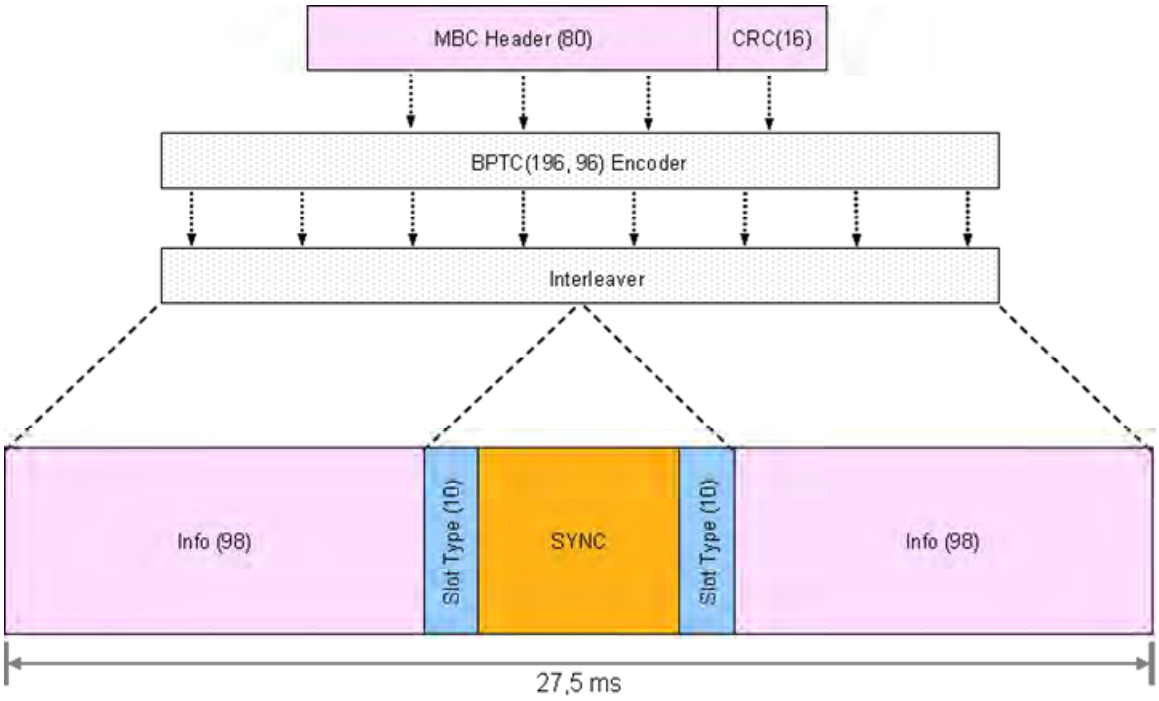


Figure 7.14: MBC header format

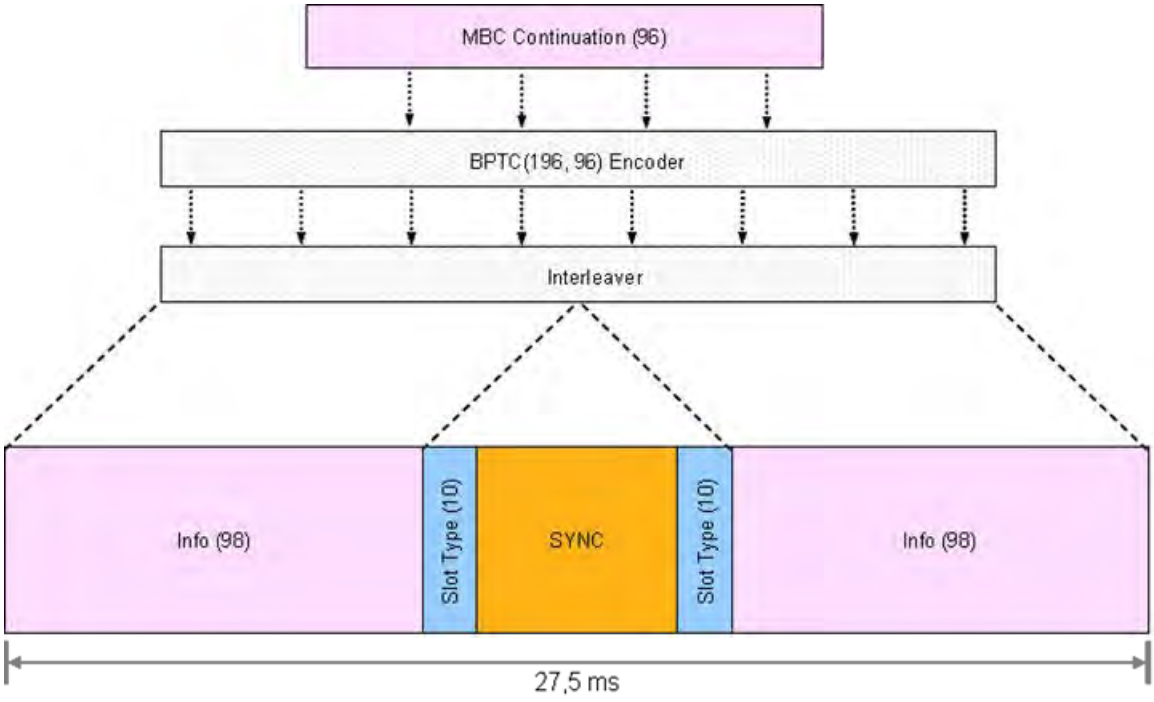


Figure 7.15: MBC intermediate block format

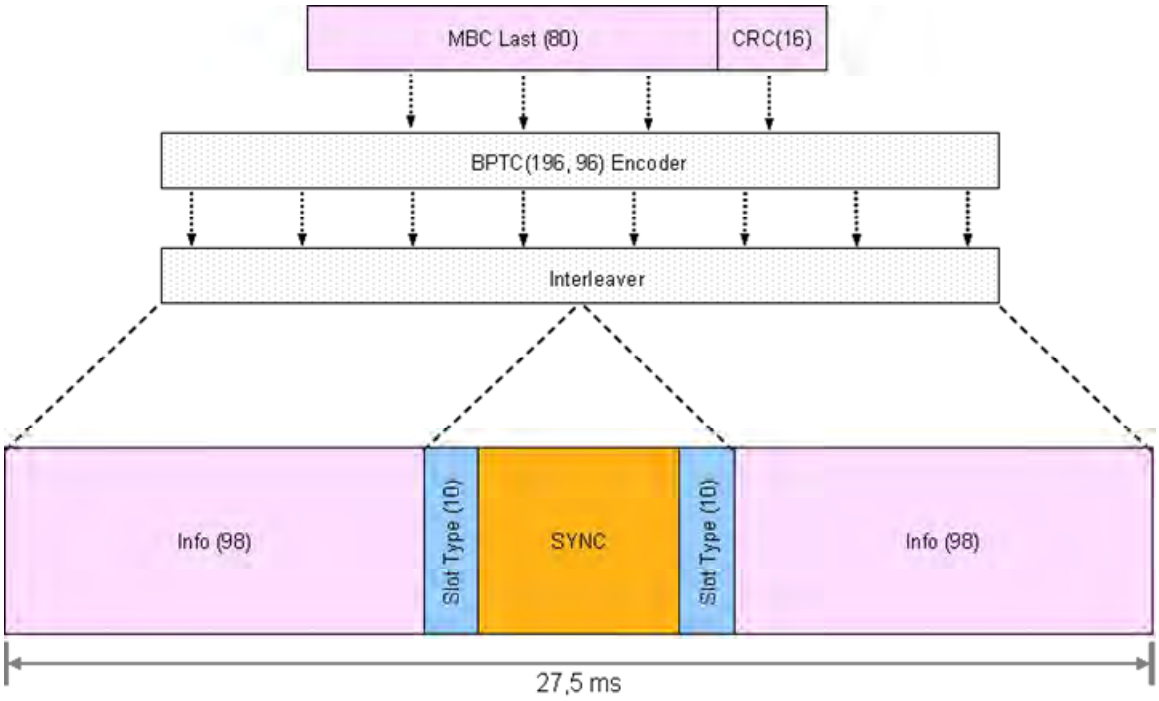


Figure 7.16: MBC last block format

Table 7.1 relates how the combination of the LB information element and the Data Type is used to distinguish the three different MBC blocks.

Table 7.1: Data Type information element definitions

Data Type	LB	Comments
MBC Header	0_2	First Block
MBC Continuation	0_2	Intermediate Blocks

8 DMR Packet Data Protocol (PDP)

8.0 DMR Packet Data Protocol (PDP) - Introduction

This clause defines DMR Packet Data Protocol (PDP) for packet data operation. Data messages of arbitrary length are transferred over the DMR Air Interface using a packet technique. The present document supports the following layer 3 protocols:

- Internet Protocol.
- Short Data Protocol.

8.1 Internet Protocol

The present document supports the Internet Protocol version 4 (IPv4).

NOTE: For detailed description refer to IETF RFC 791 [6].

DMR PDP extends DMR to act as an IP subnet. This enables application programmers to build their applications in a well standardized environment.

The implementation of BS IP routing and relaying as well as the connection to external networks is outside the scope.

Ipv4 provides a connectionless, best-effort datagram delivery between two service access points. IPv4 protocol is called on by host-to-host protocols (e.g. TCP, UDP) in an internet environment. IPv4 calls on Air Interface protocol to carry the IP datagram over the air.

8.2 Datagram fragmentation and re-assembly

8.2.0 Datagram fragmentation and re-assembly - Introduction

Air Interface Protocol carries the IP datagrams over the air. It provides fragmentation and assembly, error correction and detection, confirmed delivery, and confidentiality over the air.

An IP datagram that is bigger than a maximum length is first split into fragments. Each fragment is then formed into a single packet consisting of a sequence of data blocks 1 to m preceded by one or two header blocks. Each block is protected by its own FEC code. The decomposition of an IP datagram is shown in figure 8.1 where each data packet has one header block. The transmission may use single slot or dual slot data capability.

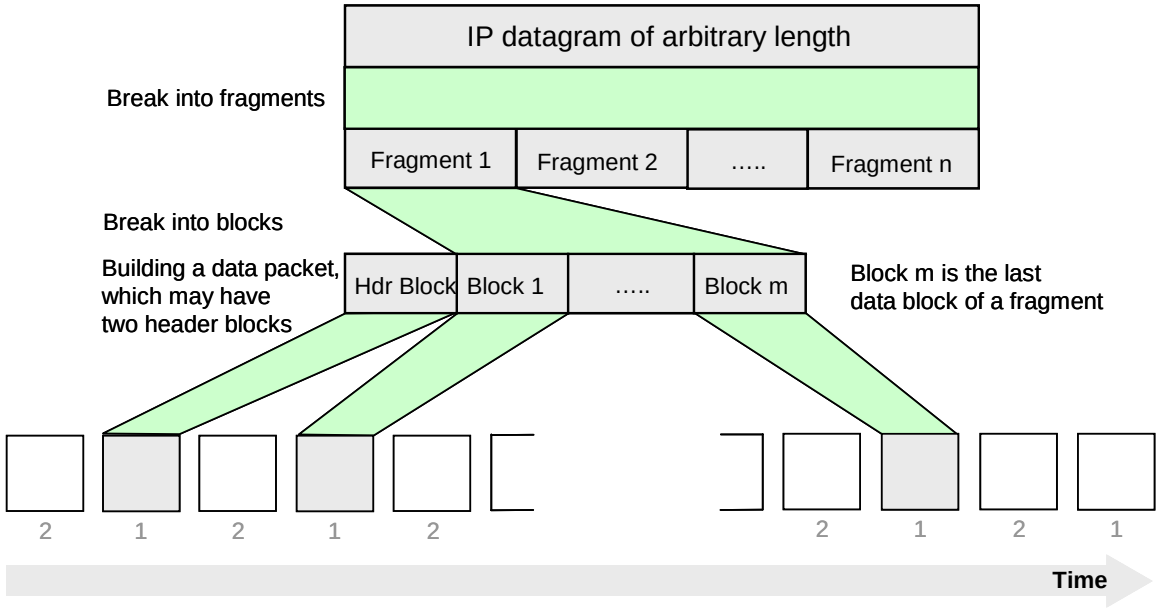


Figure 8.1: Decomposition of datagram into packets

The maximum number of fragments of a single datagram is not bounded. Each fragment length may be variable but shall not exceed a maximum length of n_DFragMax octets. Each fragment is in turn split into blocks with each block containing a different number of data octets as shown in table 8.1.

Table 8.1: Octets per data block

Confirmed/ Unconfirmed	FEC coding rate	Data octets per block
Confirmed	Rate ½	10
Confirmed	Rate ¾	16
Confirmed	Rate 1	22
Unconfirmed	Rate ½	12
Unconfirmed	Rate ¾	18
Unconfirmed	Rate 1	24

There is a special block called a header block. One or two header block(s) are sent at the beginning of a data packet.

The maximum number of blocks in a packet, including the header block(s), N_BlockMax is either:

a) for rate ½ coded confirmed data:

$$N\_BlockMax = \left\lceil \frac{N\_DFragMax - 6}{10} \right\rceil + 1 + N\_HeaderBlocks$$

b) for rate ¾ coded confirmed data:

$$N\_BlockMax = \left\lceil \frac{N\_DFragMax - 12}{16} \right\rceil + 1 + N\_HeaderBlocks$$

c) for rate 1 coded confirmed data:

$$N\_BlockMax = \left\lceil \frac{N\_DFragMax - 18}{22} \right\rceil + 1 + N\_HeaderBlocks$$

d) for rate ½ coded unconfirmed data:

$$N\_BlockMax = \left\lceil \frac{N\_DFragMax - 8}{12} \right\rceil + 1 + N\_HeaderBlocks$$

e) for rate ¾ coded unconfirmed data:

$$N\_BlockMax = \left\lceil \frac{N\_DFragMax - 14}{18} \right\rceil + 1 + N\_HeaderBlocks$$

f) for rate 1 coded unconfirmed data:

$$N\_BlockMax = \left\lceil \frac{N\_DFragMax - 20}{24} \right\rceil + 1 + N\_HeaderBlocks$$

The MS and BS shall have storage for a fragment of at least n_DFragMax octets.

The header block has 4 bit Fragment Sequence Number (FSN) field that helps in reassembly of fragments. For multi-fragment confirmed data the MSB of the FSN is a flag that indicates the last fragment and the least significant 3 bits are used for the sequence number of the fragments. It starts from value 000_2 and cycles from 001_2 to 111_2. The value 000_2 is used only for the first fragment.

The example in table 8.2 shows FSN coding of a multi-fragment confirmed datagram having 14 fragments.

Table 8.2: FSN coding scheme

Fragment	1	2	3	4	5	6	7	8	9	10	11	12	13	14
FSN	0000_2	0001_2	0010_2	0011_2	0100_2	0101_2	0110_2	0111_2	0001_2	0010_2	0011_2	0100_2	0101_2	1110_2

8.2.1 Header block structure

8.2.1.0 Header block structure - Introduction

The header blocks are distinguished from other bursts by the "Data Type" field of the "Slot Type" equal to "Data Header". The header block contains 10 octets of address and control information, followed by 2 octets of a header CRC error detection code. The header CRC is calculated from the first 10 octets of address and control using the cyclical redundant coding procedure commonly referred to as CRC-CCITT as described in clause B.3.8.

Before the BPTC(196,96) encoder, the appropriate Data Type CRC Mask as defined in clause B.3.12 shall be applied to the 16 bit CRC.

The structure of the first header block is shown in the figure 8.2. The first header block is always present in a data packet (including proprietary data packet).

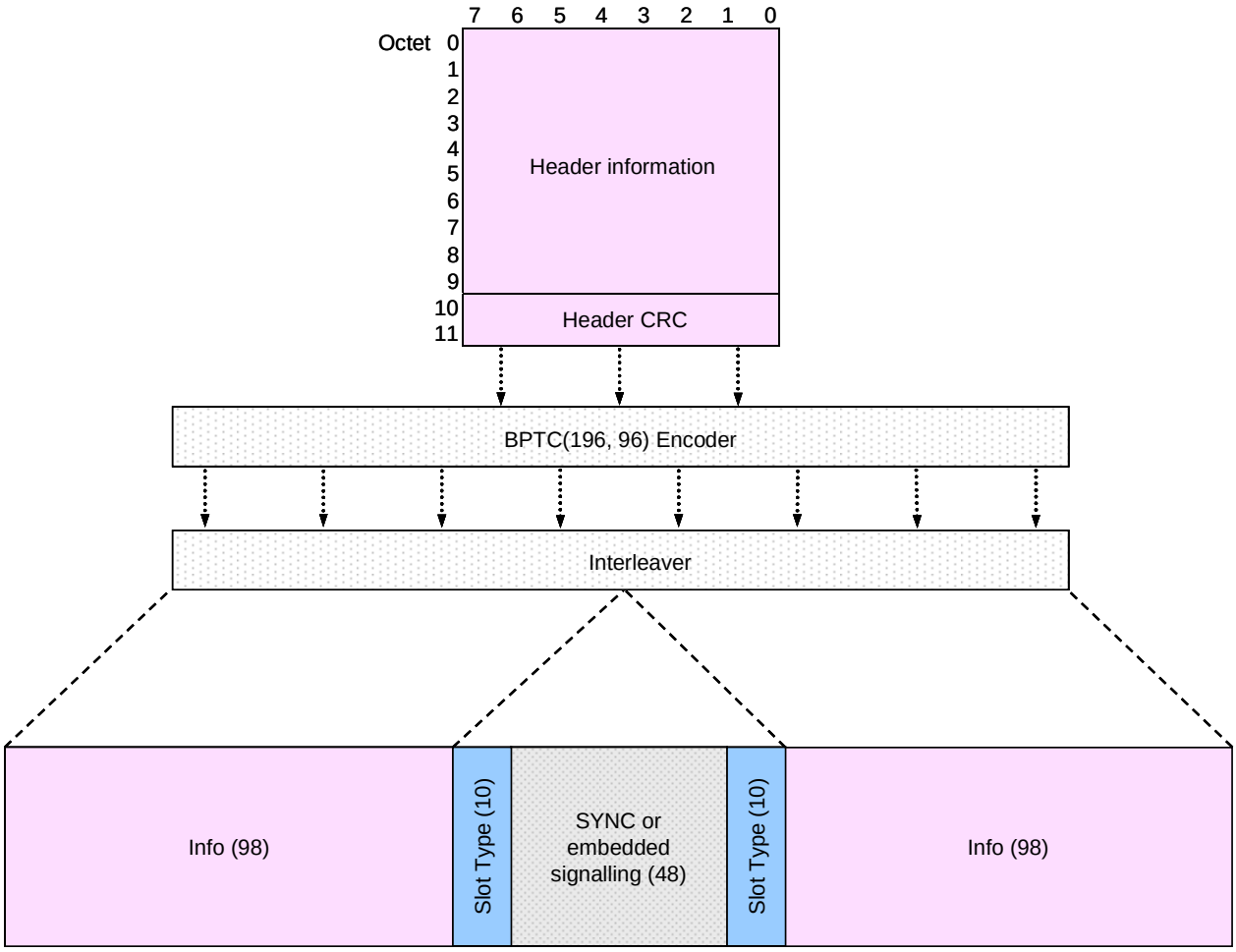


Figure 8.2: Structure of the generic first header block

8.2.1.1 Unconfirmed data Header

The structure of the first header block for an Unconfirmed packet is shown in figure 8.3. Bit 4 of octet 0 shall be the most significant bit of the 5 bit Pad Octet Count (POC) information element.

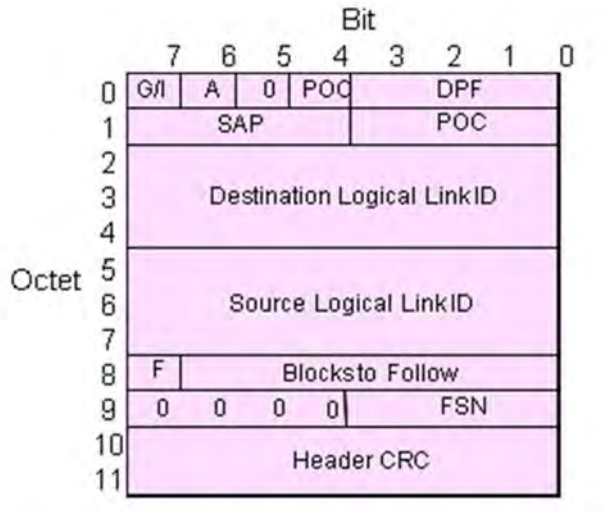


Figure 8.3: Specific first header block for unconfirmed packet

8.2.1.2 Confirmed data header

The structure of the first header block for a confirmed packet is shown in figure 8.4. Bit 4 of octet 0 shall be the most significant bit of the 5 bit Pad Octet Count (POC) information element.

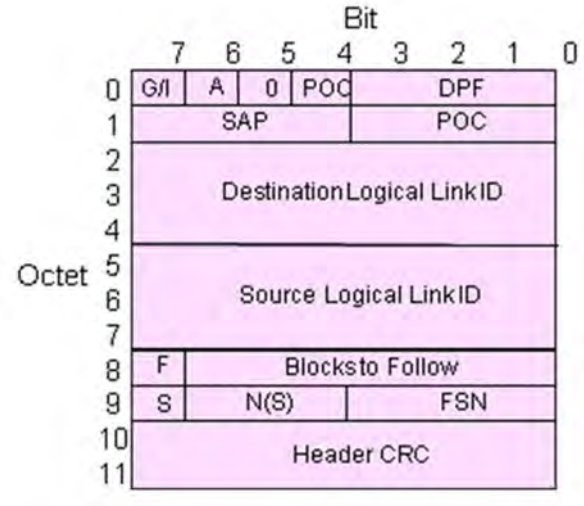


Figure 8.4: Specific first header block for confirmed packet

8.2.1.3 Response data header

The structure of the first header block for a response packet is shown in figure 8.5.

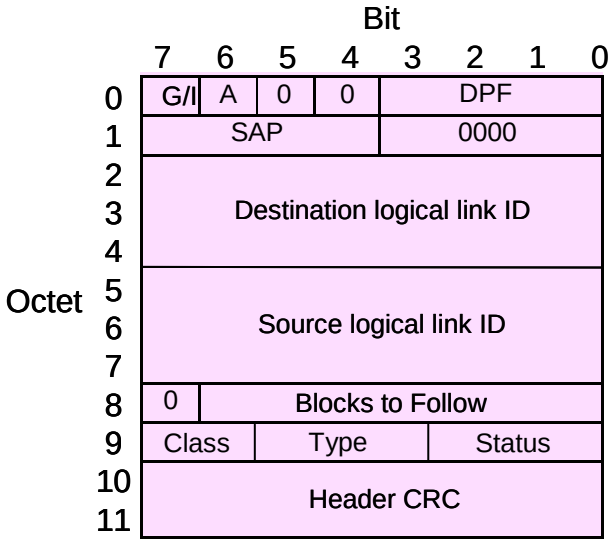


Figure 8.5: Specific first header block for response packet

8.2.1.4 Proprietary data header

A proprietary data packet uses any data header block as its first header block. It also has a second header block. The presence of second header block is indicated by the specific value (= 9) of the Service Access Point (SAP) information element of the first header. The structure of the second header block is shown in the figure 8.6.

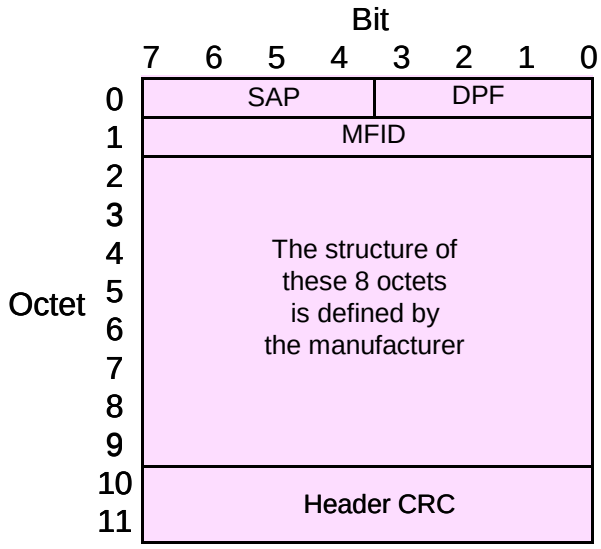


Figure 8.6: Second header block of a proprietary packet

8.2.1.5 Status/precoded short data header

The structure of the first header block for a status/precoded short data packet is shown in figure 8.7. Bits 5 and 4 of octet 0 shall be the 2 most significant bits of the 6 bit AB information element. Bits 1 and 0 of octet 8 shall be the 2 most significant bits of the 10 bit Status/Precoded information element.

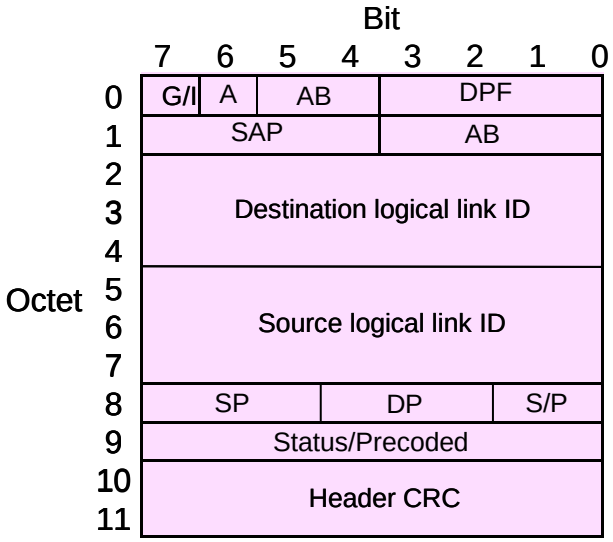


Figure 8.7: Specific first header block for status/precoded short data packet

8.2.1.6 Raw short data header

The structure of the first header block for a raw short data packet is shown in figure 8.8. Bits 5 and 4 of octet 0 shall be the 2 most significant bits of the 6 bit AB information element.

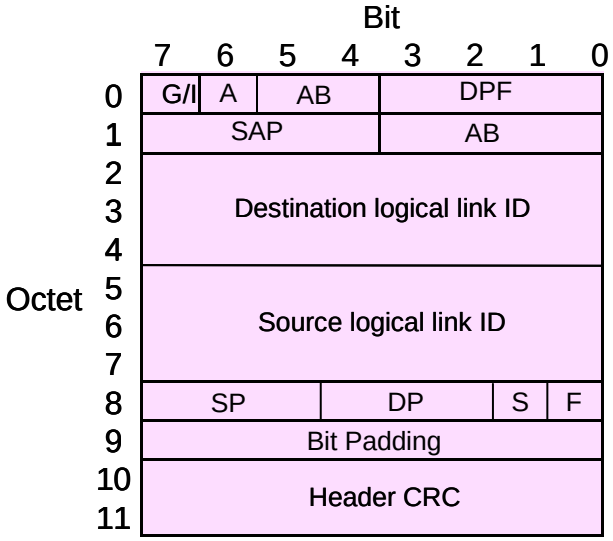


Figure 8.8: Specific first header block for raw short data packet

8.2.1.7 Defined short data header

The structure of the first header block for a defined short data packet is shown in figure 8.9. Bits 5 and 4 of octet 0 shall be the 2 most significant bits of the 6 bit AB information element.

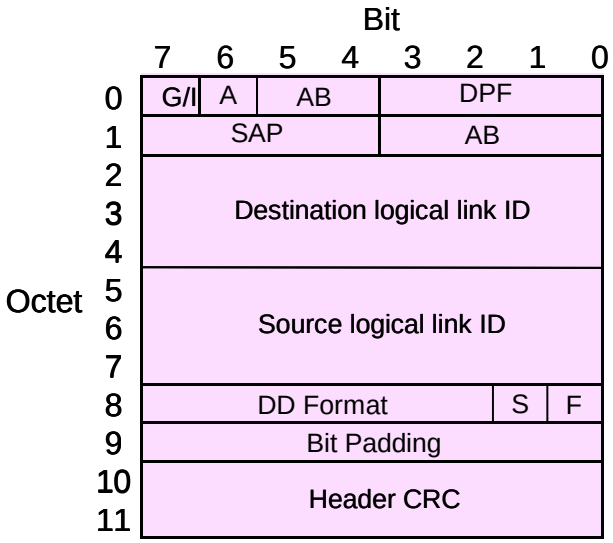


Figure 8.9: Specific first header block for defined short data packet

8.2.1.8 Unified Data Transport (UDT) data header

The structure of the first header block UDT data packet is shown in figure 8.10.

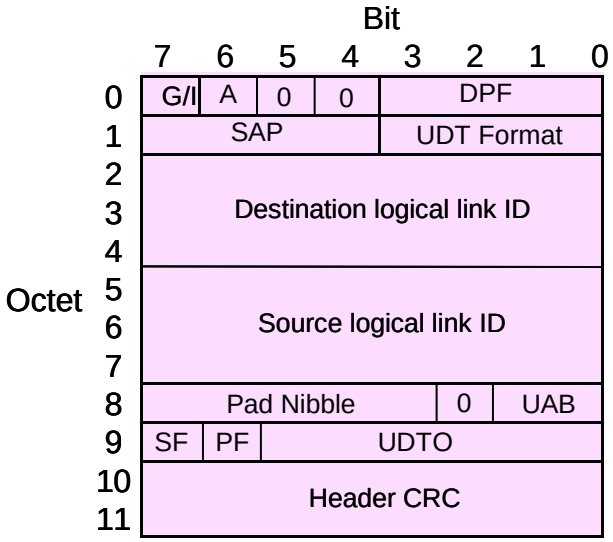


Figure 8.10: Specific first header block for UDT data packet

8.2.2 Data block structure

8.2.2.0 Data block structure - Introduction

A data packet is protected by a 32-bit CRC over the data contents to allow the recipient to determine if the packet has been received without error. This CRC is positioned at the end of the packet, as the last four octets in the last block of the packet. This is referred to as the packet CRC and described in clause B.3.9. Additional octets may be appended to the end of the data in the packet, but before the CRC, to extend the total packet length to exactly fill all of the blocks in the packet. The number of additional octets is indicated by the Pad Octet Count field of the first header block. The service required to process the data packet is indicated by the SAP of the preceding header. The value of SAP for IP based packet is 4.

The number of blocks in the packet excluding the first header block is indicated in the header block by the field blocks to follow.

Data may be sent with either confirmed delivery or unconfirmed delivery. Confirmed delivery is used to require the recipient of the packet to send an acknowledgment of receipt. Unconfirmed delivery is used if the originator of the packet does not require an acknowledgment. The distinction between confirmed and unconfirmed packet is indicated in the Data Packet Format (DPF) field of the header block.

8.2.2.1 Unconfirmed data block structure

The unconfirmed data blocks follow an unconfirmed data header. The data type information element of the SLOT PDU may be either "rate ½ coded", or "rate ¾ rate coded" or "rate 1 coded". During a data transmission the data type information element in the SLOT PDU of the data blocks and therefore the coding rate of the data blocks shall not change. Unconfirmed data blocks using rate ½ coding are packets with 12 octets in each block, where each block is protected with a BPTC(196, 96) code. The last block shall contain a data CRC in the last four octets. The formula for the number of octets of user data is as follows:

$$\text{Number Data Octets} = 12 \times (\text{Blocks To Follow - no. of additional headers}) - 4 - \text{Pad Octet Count}$$

The Unconfirmed data block format when using rate ½ coding is shown in figure 8.11.

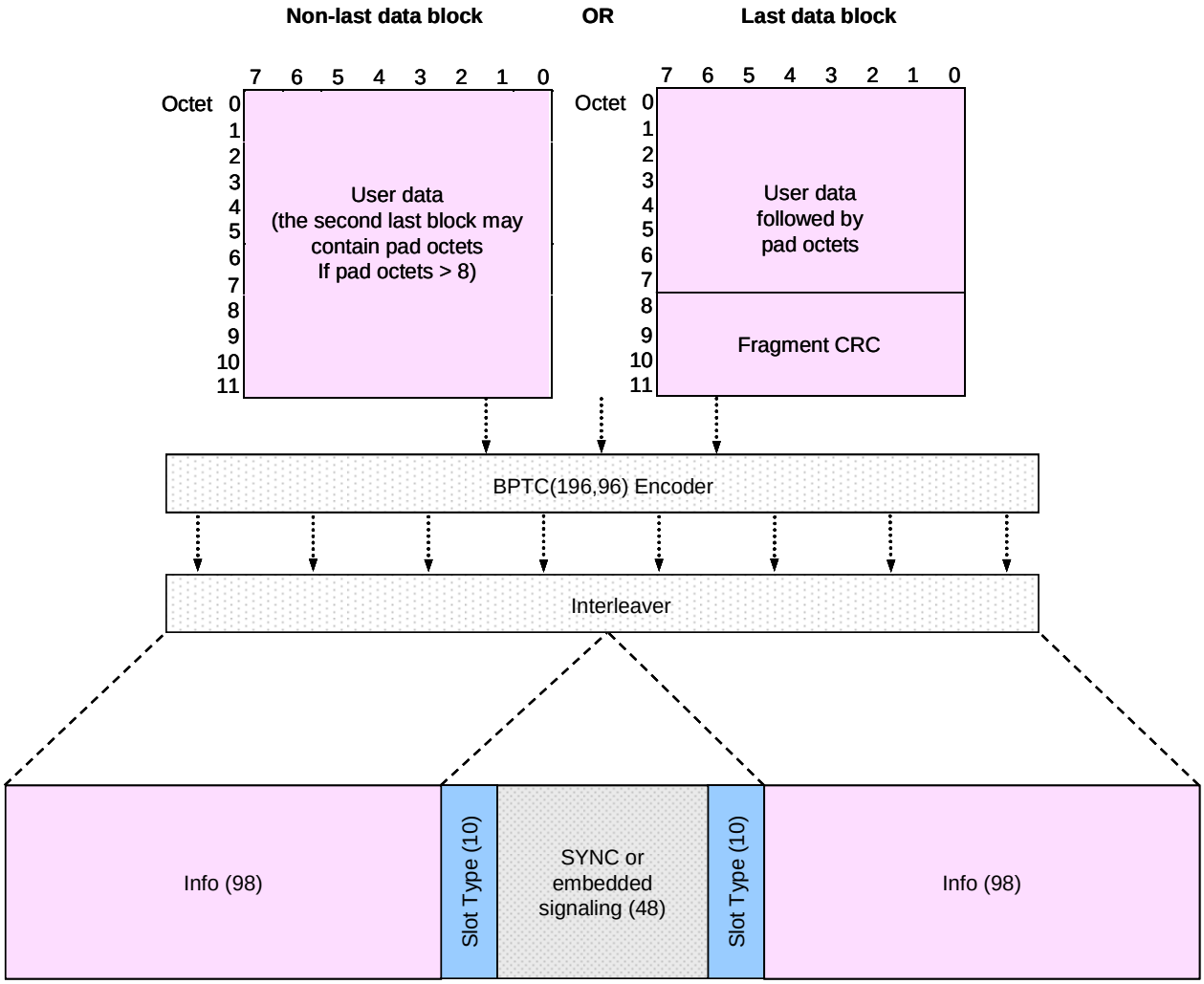


Figure 8.11: Unconfirmed rate ½ coded data block format

Unconfirmed data blocks using rate ¾ coding are packets with 18 octets in each block, where each block is protected with a rate ¾ Trellis code. The Last Block shall contain a data CRC in the last four octets. The formula for the number of octets of user data is as follows:

Number Data Octets = 18 × (Blocks To Follow - no. of additional headers) - 4 - Pad Octet Count

The Unconfirmed data block format when using rate ¾ coding is shown in figure 8.12.

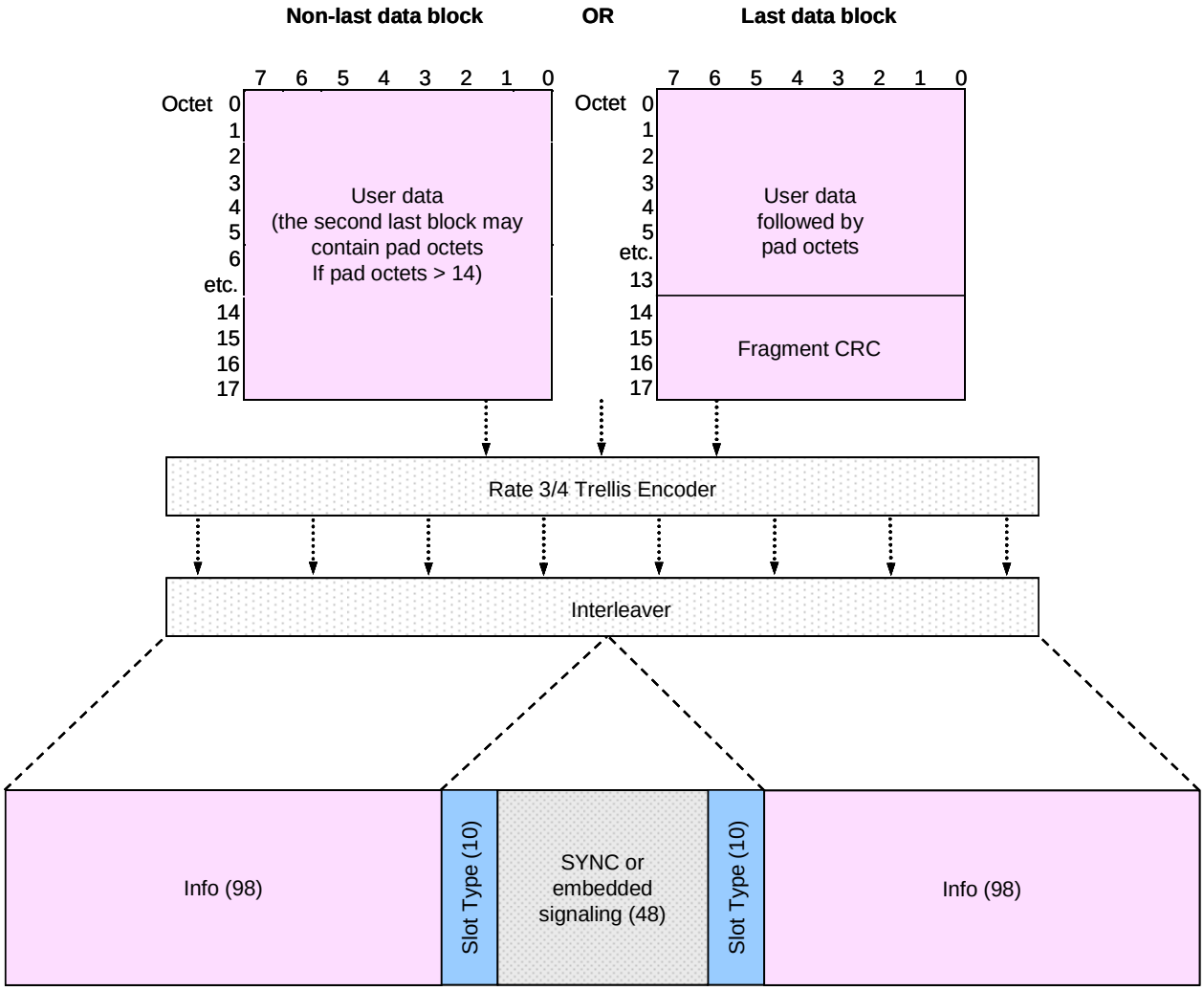


Figure 8.12: Unconfirmed rate ¾ coded data block format

Unconfirmed data blocks using rate 1 coding are packets with 24 octets in each block, where each block is uncoded. The Last Block shall contain a data CRC in the last four octets. The formula for the number of octets of user data is as follows:

Number Data Octets = 24 × (Blocks To Follow - no. of additional headers) - 4 - Pad Octet Count

The Unconfirmed data block format when using rate 1 coding is shown in figure 8.13.

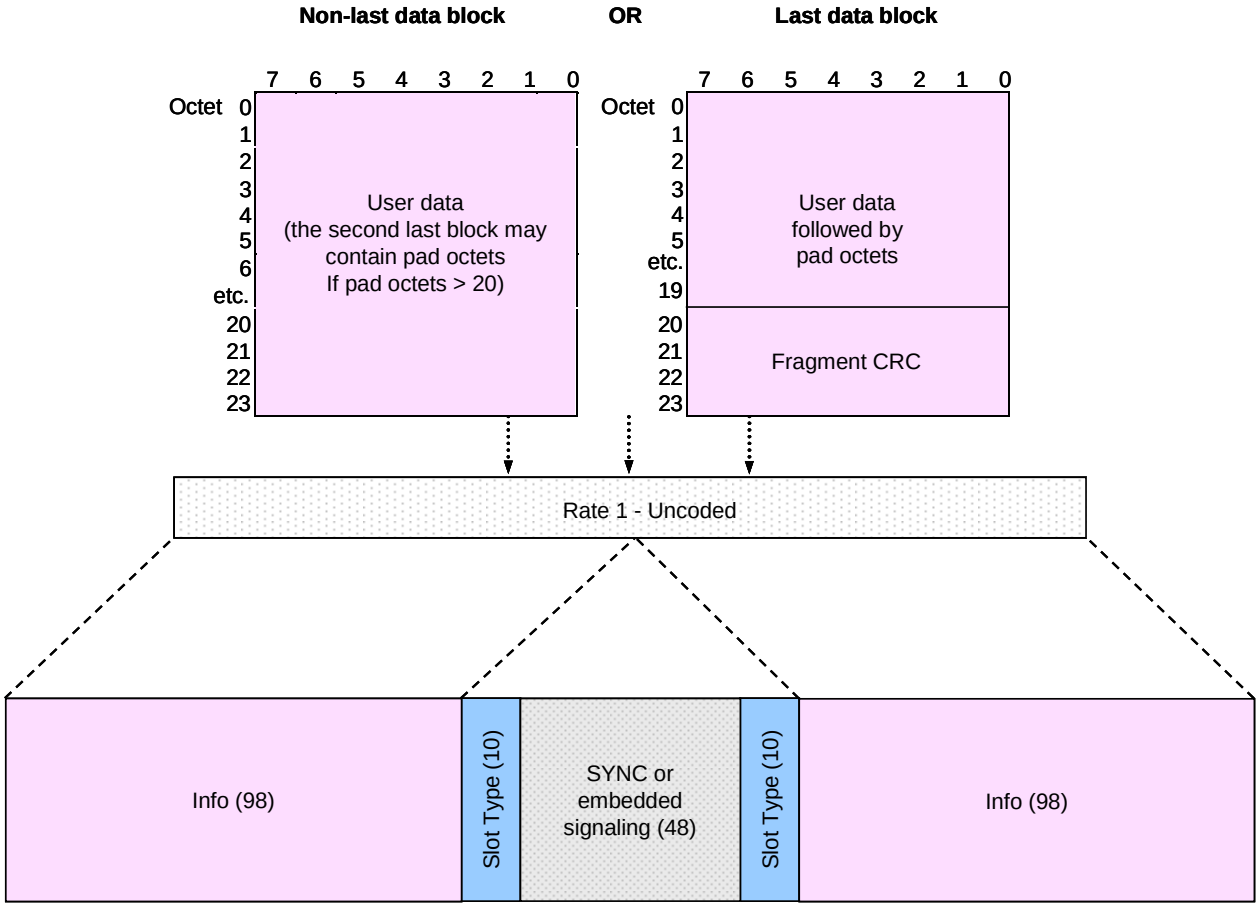


Figure 8.13: Unconfirmed rate 1 coded data block format

8.2.2.2 Confirmed data block structure

The Confirmed data blocks follow a Confirmed Data Header. The Data Type information element of the SLOT PDU may be either "rate ½ coded", or "rate ¾ rate coded" or "rate 1 coded". During a data transmission the Data Type information element of the SLOT PDU of the data blocks and therefore the coding rate of the data blocks shall not change. In the case of confirmed delivery using rate ¾ coding, a data block contains 16 octets of data, and two octets of control data (a 7-bit block serial number and a 9-bit CRC). The 9-bit CRC is calculated over 7-bit data block serial number concatenated with user data in the block. Each block in the packet, when using rate ¾ coding, is protected with a rate ¾ Trellis code. The formula for the number of octets of user data is as follows:

Number Data Octets = 16 × (Blocks To Follow - no. of additional headers) - 4 - Pad Octet Count

The Confirmed data block format when using rate ¾ coding is shown in figure 8.14.

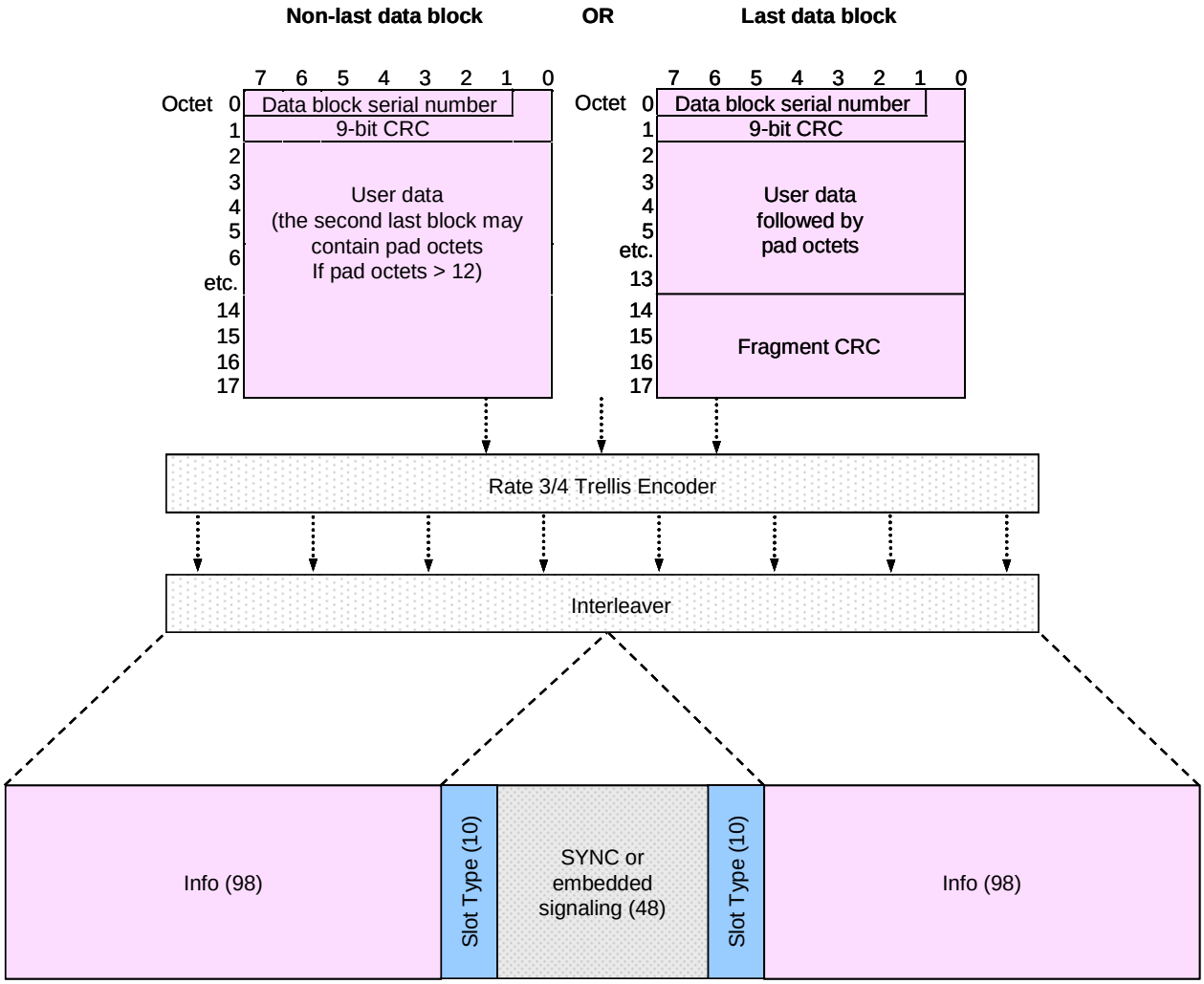


Figure 8.14: Confirmed rate ¾ coding data block format

In the case of confirmed delivery using rate ½ coding, a data block contains 10 octets of data, and two octets of control data (a 7-bit block serial number and a 9-bit CRC). The 9-bit CRC is calculated over 7-bit data block serial number concatenated with user data in the block.

Before the FEC encoder, the appropriate Data Type CRC Mask as defined in clause B.3.12 of the present document shall be applied to the 9 bit CRC. Each block in the packet, when using rate ½ coding, is protected with a BPTC(196, 96) code. The formula for the number of octets of user data is as follows:

Number Data Octets = 10 × (Blocks To Follow - no. of additional headers) - 4 - Pad Octet Count.

The Confirmed data block format when using rate ½ coding is shown in figure 8.15.

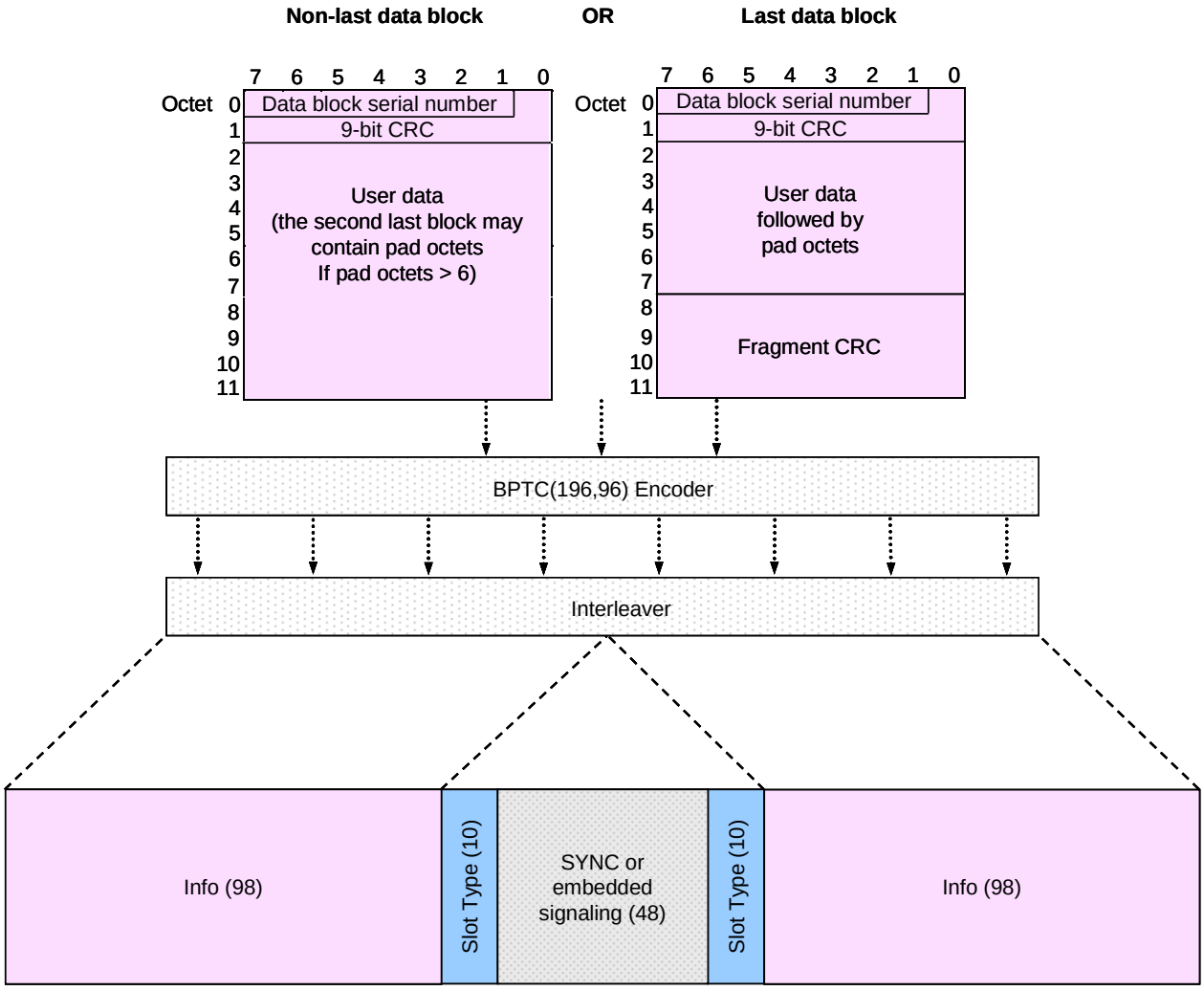


Figure 8.15: Confirmed rate ½ coding data block format

In the case of confirmed delivery using rate 1 coding, a data block contains 22 octets of data, and two octets of control data (a 7-bit block serial number and a 9-bit CRC). The 9-bit CRC is calculated over 7-bit data block serial number concatenated with user data in the block.

Before the FEC encoder, the appropriate Data Type CRC Mask as defined in clause B.3.12 of the present document shall be applied to the 9-bit CRC. Each block in the packet, when using rate 1 coding, is unprotected. The formula for the number of octets of user data is as follows:

Number Data Octets = 22 × (Blocks To Follow - no. of additional headers) - 4 - Pad Octet Count.

The Confirmed data block format when using rate 1 coding is shown in figure 8.16.

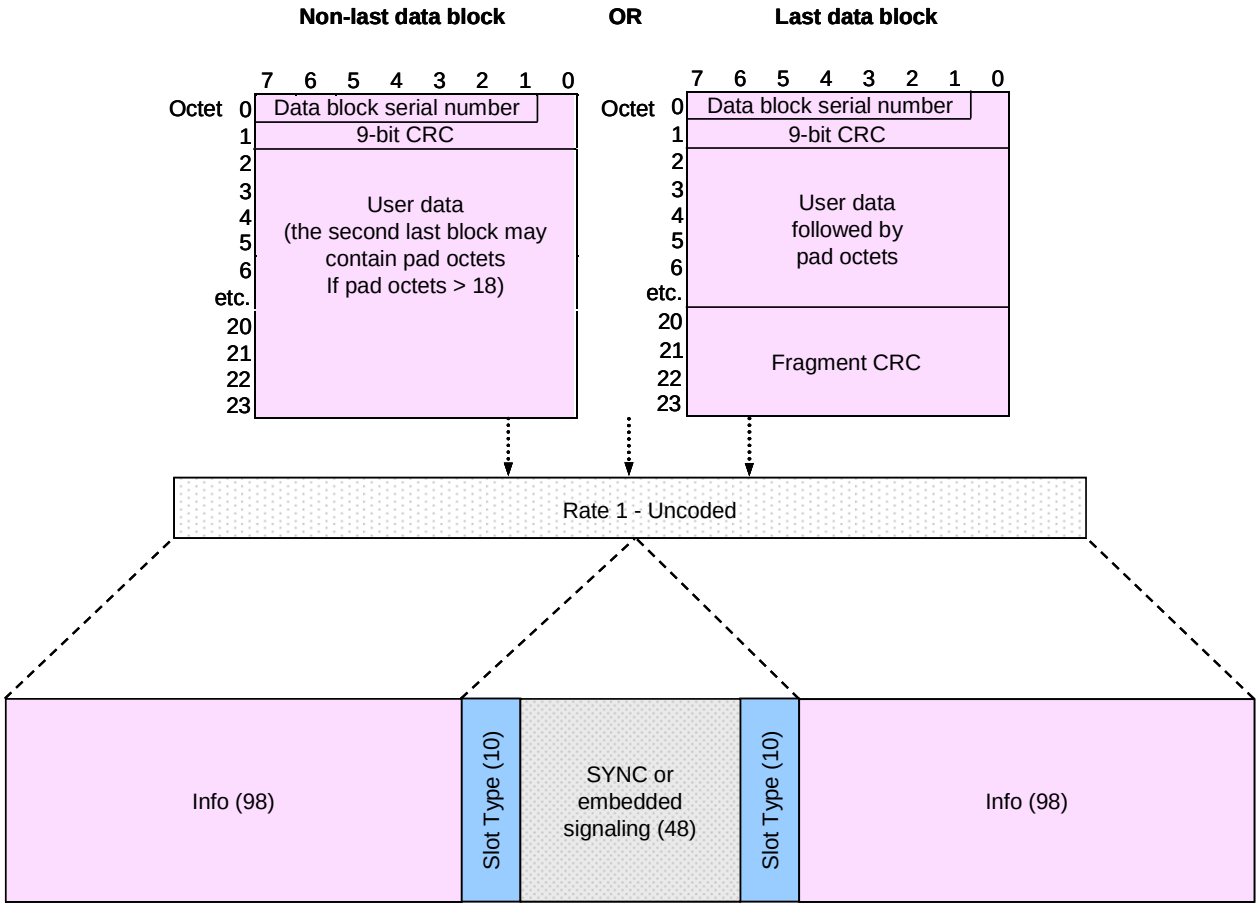


Figure 8.16: Confirmed rate 1 coding data block format

The block serial number and CRC allow the recipient to distinguish the data blocks that were received correctly. In case of confirmed delivery, the recipient sends an acknowledgment back to the sender to request a retransmission of only the corrupted blocks. This is called selective ARQ.

The block serial number is used to distinguish a corrupted block. The serial number of the data blocks of a packet start at 0 and increment up to (Blocks To Follow - numbers of headers). On subsequent retries, the sender sends the corrupted blocks with their serial numbers.

8.2.2.3 Response packet format

The Response packet is used to confirm the delivery of confirmed data packets. The recipient sends a response packet when "A" bit (in the header block) of the received packet is set. The response packet header block is shown in figure 8.5.

The Class, Type and Status field in the header block of a response packet specifies the meaning of the response as shown in table 8.3.

In the case where blocks are to be selectively retried, the Class field shall be set to 10_2, and subsequent blocks of additional information are appended to the header block. The number of blocks is indicated in the Blocks To Follow field. The format for data blocks is shown in figure 8.17 for the case where only a single data block follows the response packet header. It contains selective retry flags for up to 64 blocks. If more flags are necessary, then two blocks may be used and flags for up to 127 blocks are sent. The data blocks of the Response packet are distinguished from other bursts by the "Data Type" field of the "Slot Type" equal to "Unconfirmed Data Continuation".

A flag bit is set to 1_2 to indicate the receipt of the corresponding block, and is set to 0_2 to indicate that the block should be retried. The position of a flag bit indicates its corresponding block. Unused flag bits, i.e. the flag bits whose position number is more than the number of blocks used in the packet shall be set to 1_2.

Table 8.3: Response Packet Class, Type, and Status definitions

Class	Type	Status	Message	Comment
00_2	001_2	NI	ACK	All blocks of all packets up to NI are successfully received
01_2	000_2	NI	NACK	Illegal format, NI may have no real meaning
01_2	001_2	NI	NACK	Packet CRC of a packet with NI failed
01_2	010_2	NI	NACK	Memory of the recipient is full
01_2	011_2	FSN	NACK	The received FSN is out of sequence
01_2	100_2	NI	NACK	Undeliverable
01_2	101_2	VI	NACK	The received packet is out of sequence, N(S) ≠ VI or VI + 1
01_2	110_2	NI	NACK	Invalid user disallowed by the system
10_2	000_2	NI	SACK	The recipient requests the selective retry of the blocks indicated in the data block of the response packet

NOTE 1: NI is the sequence number of the last packet successfully received by the recipient.
NOTE 2: N(S) is the sequence number of the last packet sent by the sender.
NOTE 3: VI is the sequence number of the packet expected by the recipient.
NOTE 4: The FSN are the three least significant bits of the FSN field.
NOTE 5: ETSI TS 102 361-3 [12] provides bearer service specific information on the use of the information elements.

The CRC is the 32-bits CRC defined in clause B.3.9.

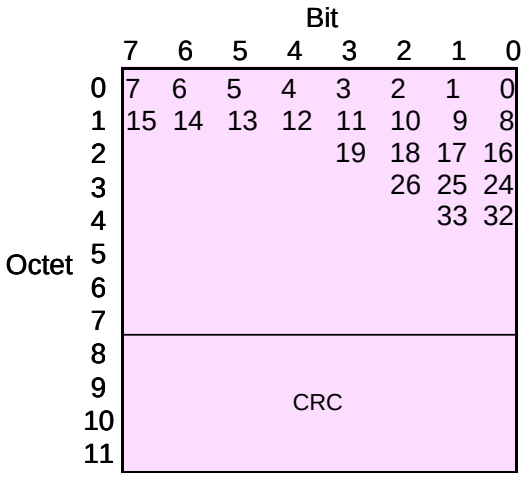


Figure 8.17: Response packet data block

8.2.2.4 Hang time for response packet

A receiving MS needs to send a response packet on receipt of a confirmed data packet. To ensure an immediate transmission of the response packet, the system reserves the channel for the response packet. This is called "data response hang time". The data response hang time is normally few bursts after the end of a data packet. In direct mode, it is the responsibility of the sending MS to indicate the start of the data response hang time by transmitting a "Data Terminator LC". The recipient should send the response politely.

To distinguish the Data Terminator LC from other bursts, the Data Type information element of the SLOT PDU shall be set to "Terminator with LC".

In repeater mode, it is the responsibility of a BS to indicate the data response hang time by transmitting a configurable number of "Data Terminator LC". To avoid collision, the repeater should also set the CACH's AT bits to BUSY during the data response hang time. A MS should send a response packet impolitely during its "data response hang time". The figure 8.18 shows the structure of the "Data Terminator LC".

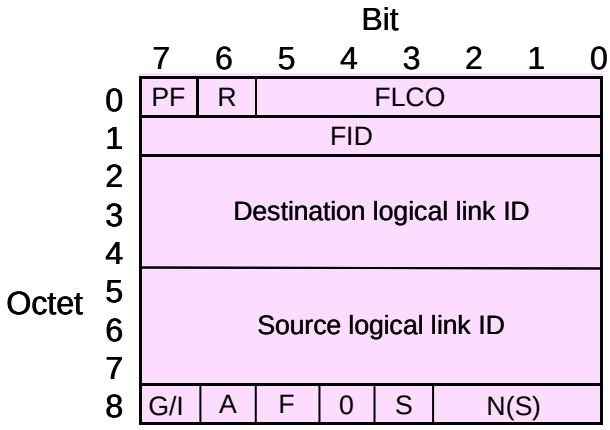


Figure 8.18: Data Terminator Link Control

8.2.2.5 Unified Data Transport (UDT) last data block structure

The UDT data blocks follow an UDT Data Header. The data type information element of the SLOT PDU shall be "rate ½ coded". Unconfirmed data blocks using rate ½ coding are packets with 12 octets in each block, where each block is protected with a BPTC (196, 96) code. The last block shall contain a data CRC in the last two octets.

The UDT last data block format when using rate ½ coding is shown in figure 8.19.

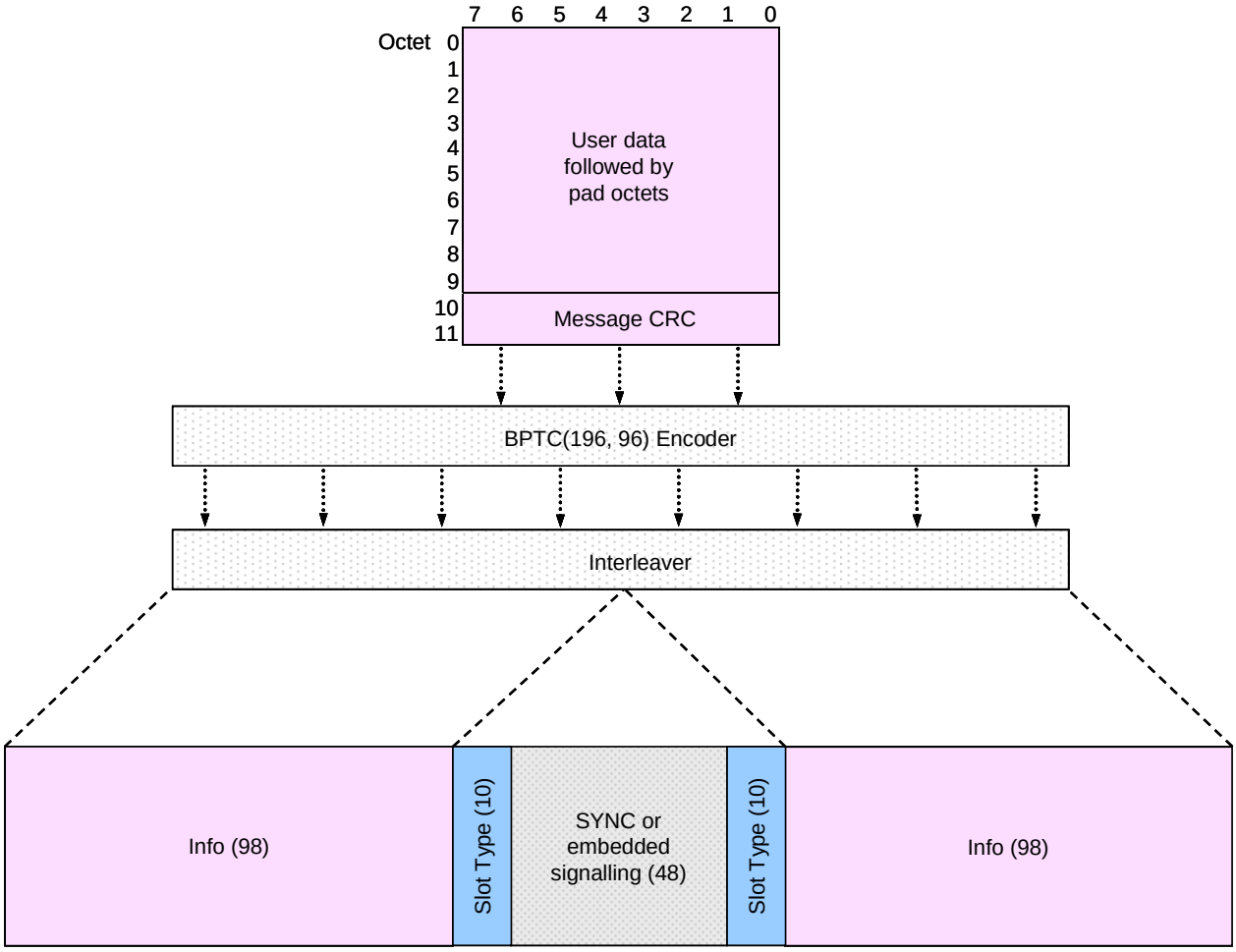


Figure 8.19: UDT last data block form

9 Layer 2 PDU description

9.0 Layer 2 PDU description - Introduction

This clause describes the PDUs which apply to the DMR Air Interface layer 2.

The following clauses contain descriptions of the PDUs and the information elements contained within them. The structure of the PDU definition represented by the tables is as follows:

- the information element column gives the name of the contained element(s);
- the element length column defines the length of the element in bits;
- the remarks column contains other information on the information element.

The elements shall be transmitted in the order specified by the burst format with the top element of the table being transmitted first (before interleaving). The content of an information element is represented by a binary value and the Most Significant Bit (MSB) of that binary value shall be transmitted first (before interleaving).

9.1 PDUs for voice bursts, general data bursts and the CACH

9.1.1 Synchronization (SYNC) PDU

Frame synchronization is the initial step to receiving a message and shall be achieved before the embedded fields can be extracted, parsed and interpreted. The TDMA protocol consists of MS sourced voice, BS sourced voice, MS sourced data or control and BS sourced data or control modes as well as TDMA direct mode time slot 1 voice, TDMA direct mode time slot 1 data, TDMA direct mode time slot 2 voice and TDMA direct mode time slot 2 data. Different frame synchronization patterns will be used to distinguish these various modes. Using the initial synchronization to carry additional information to indicate these modes will reduce the number of required dedicated signalling bits in the burst structure.

The content of the SYNC PDU is shown in table 9.1.

Table 9.1: SYNC PDU

Information element	Length	Remark
SYNC	48	The synchronization pattern is defined in table 9.2

DMR shall have a SYNC pattern as shown in table 9.2.

NOTE: The TDMA protocol defines a unique 48-bit frame SYNC patterns for voice and data, they are the symbol-wise complement of each other. The frame SYNC correlator will find a positive result for voice mode and an equal but negative result for data when running a single correlator.

Table 9.2: SYNC patterns

BS sourced													
Voice	Hex	7	5	5	F	D	7	D	F	7	5	F	7
	Binary	0111	0101	0101	1111	1101	0111	1101	1111	0111	0101	1111	0111
Data	Hex	D	F	F	5	7	D	7	5	D	F	5	D
	Binary	1101	1111	1111	0101	0111	1101	0111	0101	1101	1111	0101	1101
MS sourced													
Voice	Hex	7	F	7	D	5	D	D	5	7	D	F	D
	Binary	0111	1111	0111	1101	0101	1101	1101	0101	0111	1101	1111	1101
Data	Hex	D	5	D	7	F	7	7	F	D	7	5	7
	Binary	1101	0101	1101	0111	1111	0111	0111	1111	1101	0111	0101	0111
RC sync	Hex	7	7	D	5	5	F	7	D	F	D	7	7
	Binary	0111	0111	1101	0101	0101	1111	0111	1101	1111	1101	0111	0111
TDMA direct mode time slot 1													
Voice	Hex	5	D	5	7	7	F	7	7	5	7	F	F
	Binary	0101	1101	0101	0111	0111	1111	0111	0111	0101	0111	1111	1111
Data	Hex	F	7	F	D	D	5	D	D	F	D	5	5
	Binary	1111	0111	1111	1101	1101	0101	1101	1101	1111	1101	0101	0101
TDMA direct mode time slot 2													
Voice	Hex	7	D	F	F	D	5	F	5	5	D	5	F
	Binary	0111	1101	1111	1111	1101	0101	1111	0101	0101	1101	0101	1111
Data	Hex	D	7	5	5	7	F	5	F	F	7	F	5
	Binary	1101	0111	0101	0101	0111	1111	0101	1111	1111	0111	1111	0101
Reserved SYNC pattern													
(See note)	Hex	D	D	7	F	F	5	D	7	5	7	D	D
	Binary	1101	1101	0111	1111	1111	0101	1101	0111	0101	0111	1101	1101
NOTE: The Reserved SYNC pattern is for future use.													

9.1.2 Embedded signalling (EMB) PDU

The EMB PDU shall be used for embedded signalling within a burst. The EMB PDU has a length of 16 bits and is placed in the burst as shown in clause 6.1. The content of the EMB PDU is shown in table 9.3.

Table 9.3: EMB PDU content

Information element	Length	Remark
Colour Code (CC)	4	
Pre-emption and power control Indicator (PI)	1	
Link Control Start/Stop (LCSS)	2	
EMB parity	9	The Quadratic Residue (16,7,6) FEC shall be used as described in clause B.3.2

9.1.3 Slot Type (SLOT) PDU

The SLOT PDU shall be used for data and control. The SLOT PDU has a length of 20 bits and is placed in the burst as shown in clause 6.2. The content of the SLOT PDU is shown in table 9.4.

Table 9.4: SLOT PDU content

Information element	Length	Remark
Colour Code (CC)	4	
Data Type	4	
Slot Type parity	12	The Golay (20,8) FEC shall be used as described in clause B.3.1

9.1.4 TACT PDU

The TACT PDU shall be used for framing and status of the CACH burst. The TACT PDU has a length of 7 bits, preceding the CACH signalling. The content of the TACT PDU is shown in table 9.5.

Table 9.5: TACT PDU content

Information element	Length	Remark
Access Type (AT)	1	In continuous transmission mode, for both voice and data, the AT bit is set to 1
TDMA Channel (TC)	1	
Link Control Start/Stop (LCSS)	2	
TACT parity	3	The Hamming (7,4) FEC shall be used as described in clause B.3.5

9.1.5 Reverse Channel (RC) PDU

The RC PDU shall be used for RC signalling. The RC PDU has a length of 32 bits and embedded in the RC burst as described in clause 6.4. The content of the RC PDU is shown in table 9.6.

Table 9.6: RC PDU content

Information element	Length	Remark
RC Info Payload	4	(see note)
RC Info CRC	7	The 7 bit CRC shall be used as described in clause B.3.13
RC parity	21	Reverse Channel Single Burst BPTC FEC (clause B.2.2.2)
NOTE: The data information element is defined in ETSI TS 102 361-4 [11].		

9.1.6 Full Link Control (FULL LC) PDU

The FULL LC PDU shall be used as described in clause 7.1. The FULL LC PDU has a length of either 96 bits for header and terminator bursts or 77 bits for embedded signalling. The content of the FULL LC PDU is shown in table 9.7.

Table 9.7: FULL LC PDU content

Information element	Length	Remark
Protect Flag (PF)	1	
Reserved	1	
Full Link Control Opcode (FLCO)	6	
Feature set ID (FID)	8	The FID shall be either SFID or MFID, see clause 9.3.13
Full LC Data	56	(see note 1)
Full LC CRC	(see note 2)	Either a Reed-Solomon (12,9) FEC for header and terminator burst, as described in clause B.3.6, or a 5 bit checksum for embedded signalling, as described in clause B.3.11, shall be used
NOTE 1: The data information element is defined by the feature protocol document ETSI TS 102 361-2 [5]. NOTE 2: The length is either 24 bits for header and terminator bursts or 5 bits for embedded signalling.		

9.1.7 Short Link Control (SHORT LC) PDU

The SHORT LC PDU shall be used as described in clause 7.1. The SHORT LC PDU has a length of 36 bits. The content of the SHORT LC PDU is shown in table 9.8.

Table 9.8: SHORT LC PDU content

Information element	Length	Remark
Short LC Opcode (SLCO)	4	
Short LC Data	24	(see note)
Short LC CRC	8	The 8 bit CRC shall be used as described in clause B.3.7
NOTE: The data information element is defined in ETSI TS 102 361-2 [5].		

9.1.8 Control Signalling Block (CSBK) PDU

The CSBK PDU shall be used for signalling as described in clause 7.2. A single CSBK PDU has a length of 96 bits. This CSBK PDU is shown in table 9.9.

Table 9.9: CSBK PDU content

Information element	Length	Remark
Last Block	1	This bit shall be set to 1
Protect Flag	1	
CSBK Opcode (CSBKO)	6	
FID	8	The FID shall be either SFID or MFID, see clause 9.3.13
CSBK Data	64	See note
CSBK CRC	16	The CRC-CCITT shall be used as described in clause B.3.8
NOTE: The data information element is defined by ETSI TS 102 361-2 [5].		

9.1.9 Pseudo Random Fill Bit (PR FILL) PDU

The Pseudo Random Fill Bit (PR FILL) PDU shall be used for Idle messages as described in clause 7.3. The PR FILL PDU has a length of 96 bits. The calculation of these bits is described in clause D.2.

9.2 Data related PDU description

9.2.0 Data releated PDU description - Introduction

This clause describes the PDUs related to the packet data protocol which apply to the DMR Air Interface layer 2.

9.2.1 Confirmed packet Header (C_HEAD) PDU

The C_HEAD PDU shall be used for confirmed data delivery as described in clause 8.2.1. The C_HEAD PDU has a length of 96 bits as shown in table 9.10.

Table 9.10: C_HEAD PDU content

Information element	Length	Remark
Group or Individual	1	This bit is set to indicate that the destination LLID is for a group
Response Requested (A)	1	
Reserved	1	This bit shall be set to 0
Format	4	Data packet identification
SAP Identifier	4	
Pad Octet Count (POC)	5	
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Full Message Flag (FMF)	1	
Blocks to Follow (BF)	7	
Re-Synchronize flag (S)	1	
Send sequence Number (N(S))	3	
Fragment Sequence Number (FSN)	4	
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.2 Rate ¾ coded packet Data (R_3_4_DATA) PDU

The R_3_4_DATA PDU is used to carry user data for confirmed data delivery as described in clause 8.2.2.2. The R_3_4_DATA PDU, when used for confirmed data, has a length of 144 bits as shown in table 9.11.

Table 9.11: R_3_4_DATA PDU content for confirmed data

Information element	Length	Remark
Data Block Serial Number (DBSN)	7	
C-DATA CRC	9	The CRC-9 shall be used for DBSN and user data as described in clause B.3.10
User Data	128	The user data field may contain pad octets

The R_3_4_DATA PDU is used to carry user data for unconfirmed data delivery as described in clause 8.2.2.1. This PDU, when used for unconfirmed data, uses all 144 bits for User Data as shown in table 9.11A.

Table 9.11A: R_3_4_DATA PDU content for unconfirmed data

Information element	Length	Remark
User Data	144	The user data field may contain pad octets

9.2.3 Rate ¾ coded Last Data block (R_3_4_LDATA) PDU

The R_3_4_LDATA PDU is used as the last data block carrying user data for confirmed data delivery as described in clause 8.2.2.2. The R_3_4_LDATA PDU, when used for confirmed data, has a length of 144 bits as shown in table 9.12.

Table 9.12: R_3_4_LDATA PDU content for confirmed data

Information element	Length	Remark
Data Block Serial Number (DBSN)	7	
C-DATA CRC	9	The CRC-9 shall be used for DBSN and user data as described in clause B.3.10
User Data	96	The user data field may contain up to 12 pad octets
Message CRC	32	The 32-bit CRC shall be used for the data message as described in clause B.3.9

The R_3_4_LDATA PDU is used to carry user data for unconfirmed data delivery as described in clause 8.2.2.1. This PDU, when used for unconfirmed data, has a length of 144 bits as shown in table 9.12A.

Table 9.12A: R_3_4_LDATA PDU content for unconfirmed data

Information element	Length	Remark
User Data	112	The user data field may contain up to 14 pad octets
Message CRC	32	The 32-bit CRC shall be used for the data message as described in clause B.3.9

9.2.4 Confirmed Response packet Header (C_RHEAD) PDU

The C_RHEAD PDU shall be used as the header to confirm delivery as described in clauses 8.2.1 and 8.2.2.3. The C_RHEAD PDU has a length of 96 bits as shown in table 9.13.

Table 9.13: C_RHEAD PDU content

Information element	Length	Remark
Reserved	1	This bit shall be set to 0
Response Requested (A)	1	This bit shall be set to 0
Reserved	1	This bit shall be set to 0
Format	4	Data packet identification
SAP Identifier	4	
Pad Octet Count (POC)	5	
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Full Message Flag (FMF)	1	This bit shall be set to 0
Blocks to Follow (BF)	7	
Class	2	
Type	3	
Status	3	
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.5 Confirmed Response packet Data (C_RDATA) PDU

The C_RDATA PDU shall be used to identify data blocks to be selectively retried as described in clause 8.2.2.3. The C_RDATA PDU has a length of 96 bits as shown in table 9.14.

Table 9.14: C_RDATA PDU content

Information element	Length	Remark
Retry Flags (RF)	64	Unused flag bits and bits corresponding to blocks with numbers higher than are used in the packet, shall be set to 1_2
Response CRC	32	The 32-bit CRC shall be used as described in clause B.3.9

9.2.6 Unconfirmed data packet Header (U_HEAD) PDU

The U_HEAD PDU shall be used for unconfirmed data delivery as described in clause 8.2.1. The U_HEAD PDU has a length of 96 bits as shown in table 9.15.

Table 9.15: U_HEAD PDU content

Information element	Length	Remark
Group or Individual	1	This bit is set to indicate that the destination LLID is for a group
Response Requested (A)	1	This bit shall be set to 0
Reserved	1	This bit shall be set to 0
Format	4	Data packet identification
SAP Identifier	4	
Pad Octet Count (POC)	5	
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Full Message Flag (FMF)	1	This bit shall be set to 1
Blocks to Follow (BF)	7	
Reserved	4	These bits shall be set to 0
Fragment Sequence Number (FSN)	4	
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.7 Rate ½ coded packet Data (R_1_2_DATA) PDU

The R_1_2_DATA PDU is used to carry user data for confirmed data delivery as described in clause 8.2.2.2. The R_1_2_DATA PDU, when used for confirmed data, has a length of 96 bits as shown in table 9.15A.

Table 9.15A: R_1_2_DATA PDU content for confirmed data

Information element	Length	Remark
Data Block Serial Number (DBSN)	7	
C-DATA CRC	9	The CRC-9 shall be used for DBSN and user data as described in clause B.3.10
User Data	80	The user data field may contain pad octets

The R_1_2_DATA PDU is used to follow the unconfirmed packet header carrying only user data information as described in clause 8.2.2.1. The R_1_2_DATA PDU, when used for unconfirmed data, has a length of 96 bits and may contain pad octets as shown in table 9.15AA.

Table 9.15AA: R_1_2_DATA PDU content for unconfirmed data

Information element	Length	Remark
User Data	96	The user data field may contain pad octets

9.2.8 Rate ½ coded Last Data block (R_1_2_LDATA) PDU

The R_1_2_LDATA PDU is used as the last data block carrying user data for confirmed data delivery as described in clause 8.2.2.2. The R_1_2_LDATA PDU, when used for confirmed data, has a length of 96 bits as shown in table 9.15B.

Table 9.15B: R_1_2_LDATA PDU content for confirmed data

Information element	Length	Remark
Data Block Serial Number (DBSN)	7	
C-DATA CRC	9	The CRC-9 shall be used for DBSN and user data as described in clause B.3.10
User Data	48	The user data field may contain up to 6 pad octets
Message CRC	32	The 32-bit CRC shall be used for the data message as described in clause B.3.9

The R_1_2_LDATA PDU is used as the last data block carrying user data for unconfirmed data delivery as described in clause 8.2.2.1. The R_1_2_LDATA PDU, when used for unconfirmed data, has a length of 96 bits as shown in table 9.16.

Table 9.16: R_1_2_LDATA PDU content for unconfirmed data

Information element	Length	Remark
User Data	64	(see note)
Message CRC	32	The 32-bit CRC shall be used for the data message as described in clause B.3.9
NOTE: The user data field may contain up to 8 pad octets.		

9.2.9 Proprietary Header (P_HEAD) PDU

The P-HEAD PDU shall be used when a manufacturer wants to add its own header. The P-HEAD PDU has a length of 96 bits as shown in table 9.17.

Table 9.17: P-HEAD PDU content

Information element	Length	Remark
SAP Identifier	4	
Format	4	Data packet identification
Manufacturer's Id (MFID)	8	
Manufacturer's data	64	The syntax and semantics of these octets are proprietary
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.10 Status/Precoded short data packet Header (SP_HEAD) PDU

The SP_HEAD PDU shall be used for Status/Precoded short data delivery as described in clause 8.2.1. The SP_HEAD PDU has a length of 96 bits as shown in table 9.17A.

Table 9.17A: SP_HEAD PDU content

Information element	Length	Remark
Group or Individual	1	This bit is set to indicate that the destination LLID is for a group
Response Requested (A)	1	
Appended Blocks	6	These bits shall be set to 0
Format	4	Data packet identification
SAP Identifier	4	
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Source Port (SP)	3	
Destination Port (DP)	3	
Status/Precoded	10	
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.11 Raw short data packet Header (R_HEAD) PDU

The R_HEAD PDU shall be used for Raw short data delivery as described in clause 8.2.1. The R_HEAD PDU has a length of 96 bits as shown in table 9.17B.

Table 9.17B: R_HEAD PDU content

Information element	Length	Remark
Group or Individual	1	This bit is set to indicate that the destination LLID is for a group
Response Requested (A)	1	
Appended Blocks	6	
Format	4	Data packet identification
SAP Identifier	4	
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Source Port (SP)	3	
Destination Port (DP)	3	
Selective Automatic Repeat reQuest (SARQ)	1	
Full Message Flag	1	
Bit Padding	8	
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.12 Defined Data short data packet Header (DD_HEAD) PDU

The DD_HEAD PDU shall be used for Defined Data short data delivery as described in clause 8.2.1. The DD_HEAD PDU has a length of 96 bits as shown in table 9.17C.

Table 9.17C: DD_HEAD PDU content

Information element	Length	Remark
Group or Individual	1	This bit is set to indicate that the destination LLID is for a group
Response Requested (A)	1	
Appended Blocks	6	
Format	4	Data packet identification
SAP Identifier	4	
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Defined Data (DD)	6	Data Format
Selective Automatic Repeat reQuest (SARQ)	1	
Full Message Flag	1	
Bit Padding	8	
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.13 Unified Data Transport Header (UDT_HEAD) PDU

The UDT_HEAD PDU shall be used for UDT data delivery as described in clause 8.2.1. The UDT_HEAD PDU has a length of 96 bits as shown in table 9.17D.

Table 9.17D: UDT-_HEAD PDU content

Information element	Length	Remark
Group or Individual	1	This bit is set to indicate that the destination LLID is for a group
Response Requested (A)	1	This bit shall be set to 0
Reserved	2	These bits shall be set to 0
Format	4	Data packet identification
SAP Identifier	4	
UDT Format	4	UDT data format identification
Logical Link ID (LLID)	24	Destination
Logical Link ID (LLID)	24	Source
Pad Nibble	5	
Reserved	1	This bit shall be set to 0
UAB	2	
Supplementary Flag (SF)	1	
Protect Flag (PF)	1	
UDT Opcode (UDTO)	6	See ETSI TS 102 361-4 [11] for values
Header CRC	16	The CRC-CCITT shall be used as described in clause B.3.8

9.2.14 Unified Data Transport Last Data block (UDT_LDATA) PDU

The UDT_LDATA PDU is used as the last data block carrying user data for unconfirmed data delivery as described in clause 8.2.2.1. The U_LDATA PDU has a length of 96 bits as shown in table 9.17E.

Table 9.17E: UDT_LDATA PDU content

Information element	Length	Remark
User Data	80	(see note)
Message CRC	16	The 16-bit CRC shall be used for the data message as described in clause B.3.8
NOTE: The user data field may contain up to 10 pad octets.		

9.2.15 Rate 1 coded packet Data (R_1_DATA) PDU

The R_1_DATA PDU is used to carry user data for confirmed data delivery as described in clause 8.2.2.2. The R_1_DATA PDU, when used for confirmed data, has a length of 192 bits as shown in table 9.18.

Table 9.18: R_1_DATA PDU content for confirmed data

Information element	Length	Remark
Data Block Serial Number (DBSN)	7	
C-DATA CRC	9	The CRC-9 shall be used for DBSN and user data as described in clause B.3.10
User Data	176	The user data field may contain pad octets

The R_1_DATA PDU is used to carry user data for unconfirmed data delivery as described in clause 8.2.2.1. This PDU, when used for unconfirmed data, uses all 192 bits for user data as shown in table 9.18A.

Table 9.18A: R_1_DATA PDU content for unconfirmed data

Information element	Length	Remark
User Data	192	The user data field may contain pad octets

9.2.16 Rate 1 coded Last Data block (R_1_LDATA) PDU

The R_1_LDATA PDU is used as the last data block carrying user data for confirmed data delivery as described in clause 8.2.2.2. The R_1_LDATA PDU, when used for confirmed data, has a length of 144 bits as shown in table 9.18B.

Table 9.18B: R_1_LDATA PDU content for confirmed data

Information element	Length	Remark
Data Block Serial Number (DBSN)	7	
C-DATA CRC	9	The CRC-9 shall be used for DBSN and user data as described in clause B.3.10
User Data	144	The user data field may contain up to 18 pad octets
Message CRC	32	The 32-bit CRC shall be used for the data message as described in clause B.3.9

The R_1_LDATA PDU is used as the last data block carrying user data for unconfirmed data delivery as described in clause 8.2.2.1. The R_1_LDATA PDU, when used for unconfirmed data, has a length of 160 bits as shown in table 9.18C.

Table 9.18C: R_1_LDATA PDU content for unconfirmed data

Information element	Length	Remark
User Data	160	(see note)
Message CRC	32	The 32-bit CRC shall be used for the data message as described in clause B.3.9
NOTE: The user data field may contain up to 20 pad octets.		

9.3 Layer 2 information element coding

9.3.0 Layer 2 information element coding - Introduction

The following clauses contain descriptions of the information elements contained within layer 2 PDUs, and provide a description of what the elements represent in relation to their bit representation. The structure of the tables is as follows:

- the information element column gives the name of the element;
- the element length column defines the length of the element in bits;
- the value column denotes fixed values or a range of values;

the remarks column defines the meaning of the information element against each of its bit represented values.

9.3.1 Colour Code (CC)

The CC information element differentiates signalling that originates at another site as shown in table 9.18D.

Table 9.18D: Colour Code information element content

Information element	Length	Value	Remark
Colour Code	4	0000_2	CC 0
		etc.	etc.
		1111_2	CC 15 (see note)
NOTE: All site colour code in TDMA direct mode.			

9.3.2 Pre-emption and power control Indicator (PI)

The PI information element indicates whether the embedded signalling is associated to the same logical channel or is associated to the other logical channel. In the latter case it carries RC information as described in table 9.19.

Table 9.19: Privacy Indicator information element content

Information element	Length	Value	Remark
Pre-emption and power control Indicator	1	0_2	The embedded signalling carries information associated to the same logical channel or the Null embedded message (see note)
		1_2	The embedded signalling carries RC information associated to the other logical channel (see note)
NOTE: This is referred to Aligned channel timing (see clause 5.1.1.1); in case of Offset channel timing (see clause 5.1.1.2) both PI = 0 and PI = 1 refer to the same logical channel.			

9.3.3 LC Start/Stop (LCSS)

The LCSS information element is used for LC or CSBK signalling and indicates the start, continuation or end of a signalling as described in table 9.20.

Table 9.20: LC Start/Stop information element content

Information element	Length	Value	Remark
LC Start/Stop	2	00_2	Single fragment LC or first fragment CSBK signalling, see note
		01_2	First fragment of LC signalling
		10_2	Last fragment of LC or CSBK signalling
		11_2	Continuation fragment of LC or CSBK signalling
NOTE: There is no Single fragment LC defined for CACH signalling.			

9.3.4 EMB parity

The EMB parity has a length of 9 bits. The Quadratic Residue (16,7,6) FEC shall be used as described in clause B.3.2.

9.3.5 Feature set ID (FID)

The FID information element is used to identify one of several different "feature sets" as described in table 9.21.

Table 9.21: Feature set ID information element content

Information element	Length	Value	Remark
Feature set ID	8	00000000_2	Standardized feature set ID for the services and facilities defined in ETSI TS 102 361-2 [5] (SFID)
		00000001_2	Reserved for future standardization
		00000010_2	Reserved for future standardization
		00000011_2	Reserved for future standardization
		00000100_2	Manufacturer's specific feature set ID (MFID)
		etc.	etc.
		01111111_2	Manufacturer's specific feature set ID (MFID)
		$1xxxxxxx_2$	Reserved for future MFID's allocation (MFID)
NOTE: The FID redefines only Full LC and CSBK. It does not redefine the EMB PDU.			

9.3.6 Data Type

The Data Type information element indicates the type of data or control that is being carried in a general data burst as described in table 9.22.

Table 9.22: Data Type information element content

Information element	Length	Value	Remark
Data Type	4	0000_2	PI Header
		0001_2	Voice LC Header
		0010_2	Terminator with LC
		0011_2	CSBK
		0100_2	MBC Header
		0101_2	MBC Continuation
		0110_2	Data Header
		0111_2	Rate ½ Data
		1000_2	Rate ¾ Data
		1001_2	Idle
		1010_2	Rate 1 Data
		1011_2	Reserved for future use
		1100_2	Reserved for future use
		1101_2	Reserved for future use
		1110_2	Reserved for future use
		1111_2	Reserved for future use

9.3.7 Slot Type parity

The Slot Type parity information element has a length of 12 bits. The Golay (20,8) FEC shall be used as described in clause B.3.1.

9.3.8 Access Type (AT)

The AT information element indicates whether the next inbound slot is busy or idle as described in table 9.23.

Table 9.23: Access Type information element content

Information element	Length	Value	Remark
Access Type	1	0_2	Inbound channel is idle
		1_2	Inbound channel is busy

9.3.9 TDMA Channel (TC)

The TC information element indicates whether the next inbound and outbound burst is channel 1 or channel 2 as described in table 9.24.

Table 9.24: TDMA Channel information element content

Information element	Length	Value	Remark
TDMA Channel	1	0_2	Following outbound burst is channel 1
		1_2	Following outbound burst is channel 2

9.3.10 Protect Flag (PF)

The Protect Flag is described in table 9.25.

Table 9.25: Protect Flag information element content

Information element	Length	Value	Remark
Protect Flag (PF)	1	0_2	Reserved for future use. PF is not defined in the present document and shall be set to 0_2

9.3.11 Full Link Control Opcode (FLCO)

The FLCO information element is used to identify an "over-air" facility within a "facility set" identified by the FID as described in table 9.26.

Table 9.26: Full Link Control Opcode information element content

Information element	Length	Value	Remark
Full Link Control Opcode	6	any	Details of the FLCO element coding is defined in ETSI TS 102 361-2 [5] and ETSI TS 102 361-3 [12]

9.3.12 Short Link Control Opcode (SLCO)

The SLCO information element is used to identify the short LC message type as described in table 9.27.

Table 9.27: Short Link Control Opcode information element content

Information element	Length	Value	Remark
Short Link Control Opcode	4	any	Details of the SLCO element coding is defined in ETSI TS 102 361-2 [5]

9.3.13 TACT parity

The TACT parity information element has a length of 3 bits. The Hamming (7,4) FEC shall be used as described in clause B.3.5.

9.3.14 RC parity

The RC parity information element has a length of 21 bits. The variable BPTC FEC shall be used as described in clause B.2.2.

9.3.15 Group or Individual (G/I)

The G/I information element is used to indicate that the destination LLID is for a group or an individual MS as described in table 9.28.

Table 9.28: Group or Individual information element content

Information element	Length	Value	Remark
Group or Individual	1	0_2	The destination LLID is for an individual MS
		1_2	The destination LLID is for a group of MSs

9.3.16 Response Requested (A)

The A information element is used to indicate the confirmation of a data message as described in table 9.29.

Table 9.29: Response Requested information element content

Information element	Length	Value	Remark
Response Requested	1	0_2	No Response
		1_2	Response Required

9.3.17 Data Packet Format (DPF)

The DPF information element is used for data packet identification as described in table 9.30.

Table 9.30: Data packet format information element content

Information element	Length	Value	Remark
Data packet Format	4	0000_2	Unified Data Transport (UDT)
		0001_2	Response packet
		0010_2	Data packet with unconfirmed delivery
		0011_2	Data packet with confirmed delivery
		1101_2	Short Data: Defined
		1110_2	Short Data: Raw or Status/Precoded
		1111_2	Proprietary Data Packet
		others	Reserved

9.3.18 SAP identifier (SAP)

The SAPID information element in a header is used to identify the type of processing required for the following block(s). It is described in table 9.31.

Table 9.31: Service Access Point ID information element content

Information element	Length	Value	Remark
Service Access Point ID	4	0000_2	Unified Data Transport (UDT)
		0010_2	TCP/IP header compression
		0011_2	UDP/IP header compression
		0100_2	IP based Packet data
		0101_2	Address Resolution Protocol (ARP)
		1001_2	Proprietary Packet data
		1010_2	Short Data
		others	Reserved

9.3.19 Logical Link ID (LLID)

The LLID information element identifies either the source address (i.e. the MS unit) which sent the packet or the destination address (i.e. the MS unit or group of MS units) to which the packet is directed depending on the I/O information element as described in table 9.32.

Table 9.32: Logical Link ID information element content

Information element	Length	Value	Remark
Logical Link ID	24	any	Details of the LLID element coding is defined in ETSI TS 102 361-2 [5]

9.3.20 Full message flag (F)

The F information element is used in the receiver to signify that the Pad Octet Count information element indicates the amount of data being transported in the complete packet as described in table 9.33.

Table 9.33: Full Message Flag information element content

Information element	Length	Value	Remark
Full Message Flag	1	1_2	First try for the complete packet
		0_2	Subsequent tries

9.3.21 Blocks to Follow (BF)

The BF information element specifies the number of blocks in the packet not including the first header block as described in table 9.34.

Table 9.34: Blocks to Follow information element content

Information element	Length	Value	Remark
Blocks to Follow	7	any	Number of blocks to follow

9.3.22 Pad Octet Count (POC)

The POC information element specifies the number of pad octets which have been appended to the user data octets to form an integer number of blocks as described in table 9.35.

The actual number of data octets is:

a) for rate ¾ confirmed data type: 16 × (BF - no. of additional headers) - 4 - POC;

b) for rate ½ confirmed data type: 10 × (BF - no. of additional headers) - 4 - POC;

c) for rate 1 confirmed data type: 22 × (BF - no. of additional headers) - 4 - POC;

d) for rate ¾ unconfirmed data type: 18 × (BF - no. of additional headers) - 4 - POC;

e) for rate ½ unconfirmed data type: 12 × (BF - no. of additional headers) - 4 - POC;

f) for rate 1 unconfirmed data type: 24 × (BF - no. of additional headers) - 4 - POC.

Table 9.35: Pad Octet Count information element content

Information element	Length	Value	Remark
Pad Octet Count	5	any	Number of pad octets appended to the user data

9.3.23 Re-Synchronize Flag (S)

The S information element is used to re-synchronize the physical sub-layer sequence numbers as described in table 9.36.

The receiver accepts the N(S) and FSN information elements in the message if the S bit is asserted. This bit effectively disables the rejection of duplicate messages when it is asserted. It should only be asserted on specially defined registration messages. On all user data messages, it should be cleared.

Table 9.36: Re-Synchronize Flag information element content

Information element	Length	Value	Remark
Re-Synchronize Flag	1	0_2	The receiver should not sync its sequence numbers with those in the header
		1_2	The receiver should sync its sequence numbers with those in the header

9.3.24 Send sequence number (N(S))

The N(S) information element specifies the send sequence number of the packet as described in table 9.37.

This is used to identify each request packet so that the receiver may correctly order the received message segments and eliminate duplicate copies. The sequence number starts with 0 and is incremented modulo 8 for each new data packet that is transmitted. The transmitter shall not increment this counter for an automatic retry. The receiver maintains a receiver variable VI which is the sequence number of the last valid packet to be received. The receiver accepts packets with:

a) N(S) = VI or VI + 1; if

b) N(S) = VI, then the packet is a duplicate; if

c) N(S) = VI + 1, then the packet is the next one in the sequence.

Table 9.37: Send sequence number information element content

Information element	Length	Value	Remark
Send sequence number	3	any	The Packet Sequence Number of a sender. It is used for confirmed delivery of a packet

9.3.25 Fragment Sequence Number (FSN)

The FSN information element is used to consecutively number confirmed data message fragments that together make up a longer confirmed data message as described in table 9.38. It is also transmitted in single fragment unconfirmed and confirmed data messages and is also defined in table 9.38.

The most significant FSN bit for multi-fragment confirmed data messages shall be asserted for the last fragment in the chain, and shall be cleared otherwise. The three least significant bits correspond to the Fragment Sequence Number. They shall be set to 000_2 for the first fragment and shall be incremented for each subsequent message. When the number reaches 111_2 the next increment shall be 001_2 and **not** 000_2. A logical message consisting of a single physical confirmed data message (or packet) shall have a value of 1000_2 for the FSN. The example shows FSN of a datagram having 14 fragments.

EXAMPLE: FSN coding.

Fragment	1	2	3	4	5	6	7	8	9	10	11	12	13	14
FSN	0000_2	0001_2	0010_2	0011_2	0100_2	0101_2	0110_2	0111_2	0001_2	0010_2	0011_2	0100_2	0101_2	1110_2

Table 9.38: Fragment sequence number information element content

Information element	Length	Value	Remark
Fragment sequence number	4	$0xxx_2$	Subsequent confirmed data fragment with number xxx_2
		$1xxx_2$	Last confirmed data fragment with number xxx_2
		1000_2	Confirmed data single fragment
		0000_2	Unconfirmed data single fragment

9.3.26 Data Block Serial Number (DBSN)

The DBSN information element is used to identify the serial number for the data block within the packet as described in table 9.39.

On the first try these serial numbers start at 0 and increment up to M-1, where M is equal to the Blocks to Follow information element in the Header Block. On subsequent retries, not all blocks are generally included, and these serial numbers allow the transmitter to indicate which blocks are being sent.

Table 9.39: Data Block Serial Number information element content

Information element	Length	Value	Remark
Data Block Serial Number	7	any	

9.3.27 Data block CRC (CRC-9)

The Data block CRC information element has a length of 9 bits. The CRC-9 shall be used to protect the user data and DBSN information element as described in clause B.3.10.

9.3.28 Class (Class)

The Class information element is described in table 9.40. It is used together with Type and Status information elements to specify the meaning of the response, see table 8.2.

Table 9.40: Class information element content

Information element	Length	Value	Remark
Class	2	any	(see note)
NOTE: The definition will be made in ETSI TS 102 361-3 [12].			

9.3.29 Type (Type)

The Type information element is described in table 9.41. It is used together with Class and Status information elements to specify the meaning of the response, see table 8.2.

Table 9.41: Type information element content

Information element	Length	Value	Remark
Type	3	any	(see note)
NOTE: The definition will be made in ETSI TS 102 361-3 [12].			

9.3.30 Status (Status)

The Status information element is described in table 9.42. It is used together with Class and Type information elements to specify the meaning of the response, see table 8.2.

Table 9.42: Status information element content

Information element	Length	Value	Remark
Status	3	any	(see note)
NOTE: The definition will be made in ETSI TS 102 361-3 [12].			

9.3.31 Last Block (LB)

The LB information element indicates whether more blocks in a MBC are to follow, if this is the last block in an MBC or if this is the only block in a CSBK as described in table 9.43.

Table 9.43: Last Block information element content

Information element	Length	Value	Remark
Last Block	1	0_2	MBC Header or Continuation Block
		1_2	CSBK or MBC Last Block

9.3.32 Control Signalling BlocK Opcode (CSBKO)

The CSBKO information element is used to identify an "over-air" facility within a "facility set" identified by the FID as described in table 9.44.

Table 9.44: Control Signalling BlocK Opcode information element content

Information element	Length	Value	Remark
Control Signalling Block Opcode	6	any	Details of the CSBKO element coding is defined in ETSI TS 102 361-2 [5]

9.3.33 Appended Blocks (AB)

The AB information element specifies the number of appended blocks in the packet not including the first header block as described in table 9.45.

Table 9.45: Appended Blocks information element content

Information element	Length	Value	Remark
Appended Blocks	6	any	Number of appended blocks to follow

9.3.34 Source Port (SP)

The SP information element specifies the number of the source port described in table 9.46.

Table 9.46: Source Port information element content

Information element	Length	Value	Remark
Source Port	3	any	Source port number

9.3.35 Destination Port (DP)

The DP information element specifies the number of the destination port described in table 9.47.

Table 9.47: Destination Port information element content

Information element	Length	Value	Remark
Destination Port	3	any	Destination port number

9.3.36 Status/Precoded (S_P)

The S_P information element specifies the status/precoded message content as described in table 9.48.

Table 9.48: Source Port information element content

Information element	Length	Value	Remark
Status/Precoded	10	any	Message content

9.3.37 Selective Automatic Repeat reQuest (SARQ)

The SARQ information element specifies if the source requires SARQ as described in table 9.49.

Table 9.49: SARQ information element content

Information element	Length	Value	Remark
Selective Automatic Repeat reQuest	1	0_2	Source does not require SARQ
		1_2	Source does require SARQ

9.3.38 Defined Data format (DD)

The DD information element specifies data format as described in table 9.50.

Table 9.50: DD information element content

Information element	Length	Value	Remark
Defined Data format (DD)	6	000000_2	Binary
		000001_2	BCD
		000010_2	7 bit character
		000011_2	8 bit ISO/IEC 8859-1 [10]
		000100_2	8 bit ISO/IEC 8859-2 [10]
		000101_2	8 bit ISO/IEC 8859-3 [10]
		000110_2	8 bit ISO/IEC 8859-4 [10]
		000111_2	8 bit ISO/IEC 8859-5 [10]
		001000_2	8 bit ISO/IEC 8859-6 [10]
		001001_2	8 bit ISO/IEC 8859-7 [10]
		001010_2	8 bit ISO/IEC 8859-8 [10]
		001011_2	8 bit ISO/IEC 8859-9 [10]
		001100_2	8 bit ISO/IEC 8859-10 [10]
		001101_2	8 bit ISO/IEC 8859-11 [10]
		001110_2	8 bit ISO/IEC 8859-13 [10]
		001111_2	8 bit ISO/IEC 8859-14 [10]
		010000_2	8 bit ISO/IEC 8859-15 [10]
		010001_2	8 bit ISO/IEC 8859-16 [10]
		010010_2	Unicode UTF-8
		010011_2	Unicode UTF-16
		010100_2	Unicode UTF-16BE
		010101_2	Unicode UTF-16LE
		010110_2	Unicode UTF-32
		010111_2	Unicode UTF-32BE
		011000_2	Unicode UTF-32LE
		others	Reserved

9.3.39 Unified Data Transport Format (UDT Format)

The UDT Format information element specifies data format as described in table 9.51. [10]

Table 9.51: UDT Format information element content

Information element	Length	Value	Remark
Unified Data Transport Format (UDT Format)	4	0000_2	Binary
		0001_2	MS or TG Address
		0010_2	4 bit BCD
		0011_2	ISO 7-bit coded characters [9]
		0100_2	ISO 8-bit coded characters [10]
		0101_2	NMEA location coded [8]
		0110_2	IP address
		0111_2	16 bit Unicode characters
		1000_2	Custom Coded (manufacturer specific)
		1001_2	Custom Coded (manufacturer specific)
		1010_2	Mixed. Appended blocks contain an address and 16 bit UTF-16BE Unicode characters
		others	Reserved for future use

9.3.40 UDT Appended Blocks (UAB)

The UAB information element specifies the number of appended blocks in the UDT packet not including the header block as described in table 9.52.

Table 9.52: Blocks to Follow information element content

Information element	Length	Value	Remark
UDT Appended Blocks	2	any	Number of UDT appended blocks to follow

9.3.41 Supplementary Flag (SF)

The SF information element specifies the type of appended blocks in the UDT packet as described in table 9.53.

Table 9.53: Blocks to Follow information element content

Information element	Length	Value	Remark
Supplementary Flag	1	0_2	Short Data
		1_2	Supplementary Data

9.3.42 Pad Nibble

The Pad Nibble information element specifies the number of pad nibbles (4 bits) that have been appended to the user data as described in table 9.54.

Table 9 .54: Pad Nibble information element content

Information element	Length	Value	Remark
Pad Nibble	5	any	Number of pad nibbles appended to the user data

10 Physical Layer

10.1 General parameters

10.1.0 General parameters - Introduction

The DMR equipment shall comply with the essential requirements as stated in ETSI EN 300 113-2 [2] or ETSI EN 300 390-2 [4].

10.1.1 Frequency range

The radio system operates in part of the RF frequency range of 30 MHz to 1 GHz.

10.1.2 RF carrier bandwidth

The radio system operates within a 12,5 kHz RF carrier bandwidth.

10.1.3 Transmit frequency error

The maximum BS transmit frequency error from the assigned RF carrier centre shall be as defined in table 10.1.

Table 10.1: BS transmit frequency error

Frequency range	BS maximum frequency error
50 MHz to 300 MHz	±2 ppm
300 MHz to 600 MHz	±1 ppm
600 MHz to 800 MHz	±0,75 ppm
800 MHz to 1 GHz	±0,3 ppm

The maximum MS transmit frequency error from the assigned RF carrier centre shall be as defined in table 10.2.

Table 10.2: MS transmit frequency error

Frequency range	MS maximum frequency error
50 MHz to 600 MHz	±2 ppm
600 MHz to 1 GHz	±1,5 ppm

The method of measurement is defined in ETSI EN 300 113-1 [1] or ETSI EN 300 390-1 [3].

NOTE: In the 600 MHz to 1 GHz range, it is recommended that the MS is frequency locked to the BS to improve system performance.

10.1.4 Time base clock drift error

The maximum time base clock drift error for a MS not supporting TDMA direct mode shall be ±2 ppm. This error is the amount of clock drift that is acceptable during a MS transmission. Before transmission, the MS synchronizes in time with the BS. During transmission, this MS is allowed to deviate in time by the maximum time base clock drift error.

NOTE 1: This parameter limits operating distance and transmission time in 2:1-mode TDMA operation modes as defined in clause 10.2.3.1.3.

For a MS supporting TDMA direct mode the clock drift error shall not exceed the limits of -1,0 to +1,0 ppm.

NOTE 2: This is the amount of clock drift that is acceptable for an MS to keep valid channel slot timing for 10 minutes at the clock drift error extremes. Manufacturers need to be aware that this clock drift error includes both temperature stability and aging. As an example, if temperature stability is ±0,5 ppm from -30 °C to +60 °C and aging stability is ±0,5 ppm over 4 years then the part meets the clock drift error specification over a 4 year time period when operated within the -30 °C to +60 °C temperature range.

10.2 Modulation

10.2.1 Symbols

The modulation sends 4 800 symbols/s with each symbol conveying 2 bits of information.
The maximum deviation, D, of the symbol is defined as:

$$D = 3h/2T \quad (1)$$

where:

- h is the deviation index defined for the particular modulation; and
- T is the symbol time (1/4 800) in s.

10.2.2 4FSK generation

10.2.2.0 4FSK generation - Introduction

This clause describes the characteristics of the constant-envelope modulation, entitled 4FSK.

10.2.2.1 Deviation index

The deviation index, h, for 4FSK is defined to be 0,27. This yields a symbol deviation of 1,944 kHz at the symbol centre. The mapping between symbols and bits is given in table 10.3.

Table 10.3: Dibit symbol mapping to 4FSK deviation

Information bits		Symbol	4FSK deviation
Bit 1	Bit 0		
0	1	+3	+1,944 kHz
0	0	+1	+0,648 kHz
1	0	-1	-0,648 kHz
1	1	-3	-1,944 kHz

10.2.2.2 Square root raised cosine filter

A Square Root Raised Cosine Filter is implemented for 4FSK so that part of a Nyquist Raised Cosine is used for the transmit splatter filter and part is used by the receiver to reject noise. The input to the transmit splatter filter consists of a series of impulses, scaled according to clause 10.2.3.1, and separated in time by 208,33 microseconds (1/4 800 s). The method of splitting the Nyquist Raised Cosine Filter is to define the splatter filter frequency response of the Square Root Raised Cosine Filter as the square root of the Nyquist Raised Cosine Filter. The group delay of the filter is flat over the pass band for |f| < 2 880 Hz. The magnitude response of the filter is given approximately by the following formula:

$$|F(f)| = 1 \quad \text{for} \quad |f| \le 1\,920\ Hz$$

$$|F(f)| = \left|\cos\left(\pi f / 1\,920\right)\right| \quad \text{for} \quad 1\,920\ Hz < |f| \le 2\,880\ Hz$$

$$|F(f)| = 0 \quad \text{for} \quad |f| > 2\,880\ Hz \qquad (2)$$

where $|F(f)|$ = magnitude response of the Square Root Raised Cosine Filter.

NOTE: f = frequency in hertz.

10.2.2.3 4FSK Modulator

The 4FSK modulator consists of a Square Root Raised Cosine Filter, cascaded with a frequency modulator as shown in figure 10.1. The Square Root Raised Cosine Filter is described in clause 10.2.3.2.

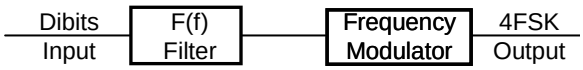


Figure 10.1: 4FSK modulator

The 4FSK modulator shall have the deviation set to provide the proper carrier phase shift for each modulated symbol. The deviation is set with a test signal consisting of the following symbol stream:

...+3 +3 -3 -3 +3 +3 -3 -3…

This test signal is processed by the modulator to create a 4FSK signal equivalent to a 1,2 kHz sine wave modulating an FM signal with a peak deviation equal to:

$\sqrt{2}$ × 1 944 Hz = 2 749 Hz.

The method of measurement employs an FM demodulator to measure both the peak positive and peak negative deviation. The audio bandwidth of the FM demodulator is set with a high pass filter corner frequency ≤ 15 Hz and a low pass filter corner frequency ≥ 3 kHz.

NOTE: The de-emphasis function is disabled on the FM demodulator.

The peak positive and peak negative deviation specification limits are 2 749 Hz ± 10 %, or 2 474 Hz to 3 024 Hz.

10.2.3 Burst timing

10.2.3.0 Burst timing - Introduction

The transmissions in a TDMA system consist of short bursts at regular intervals. The timing of these bursts is critical to the performance of a TDMA system. There are two types of bursts defined for the protocol:

- Normal Bursts; and
- RC Bursts.

Both utilize the TDMA frame and slot structure shown in figure 10.2. For some timing examples see also annex C.

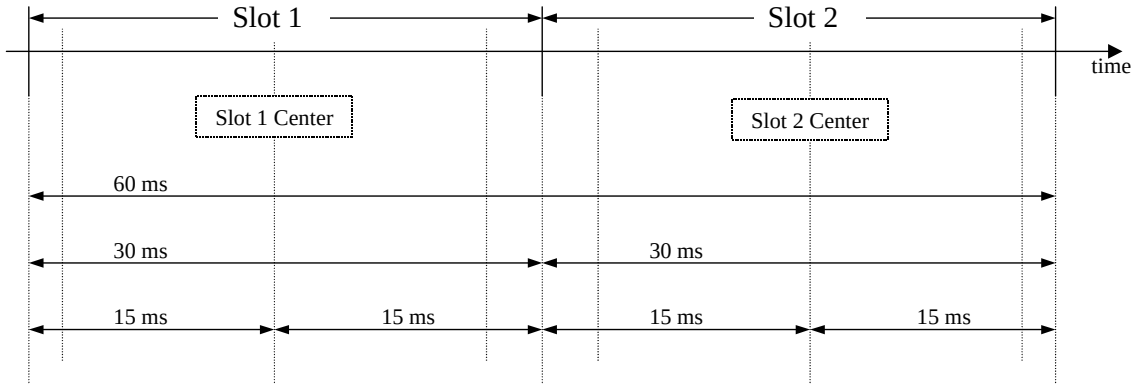


Figure 10.2: TDMA frame

Each TDMA frame is 60 ms long and consists of two 30 ms slots. Generally, one call will use Slot 1 and a different call will use Slot 2. Calls consist of a series of slots equal to the duration of the call. For systems using a BS the mobile station synchronizes to the base station. The information carried in the slot is centred on the slot centre.

10.2.3.1 Normal burst

10.2.3.1.0 Normal burst - Introduction

The Normal Burst shall be used for voice, data and control applications. It provides 264 bits of data per burst, which is a data rate of 4,4 kbit/s. This is the burst used for most applications.

10.2.3.1.1 Power ramp time

The instantaneous transmitter power levels shall be constrained to the mask given in figure 10.3. The mask assures that near-far situations will not result in co-channel inter-slot interference on the alternate or non-transmission slot. The mask also assures that the power level will be adequate for acceptable BER performance.

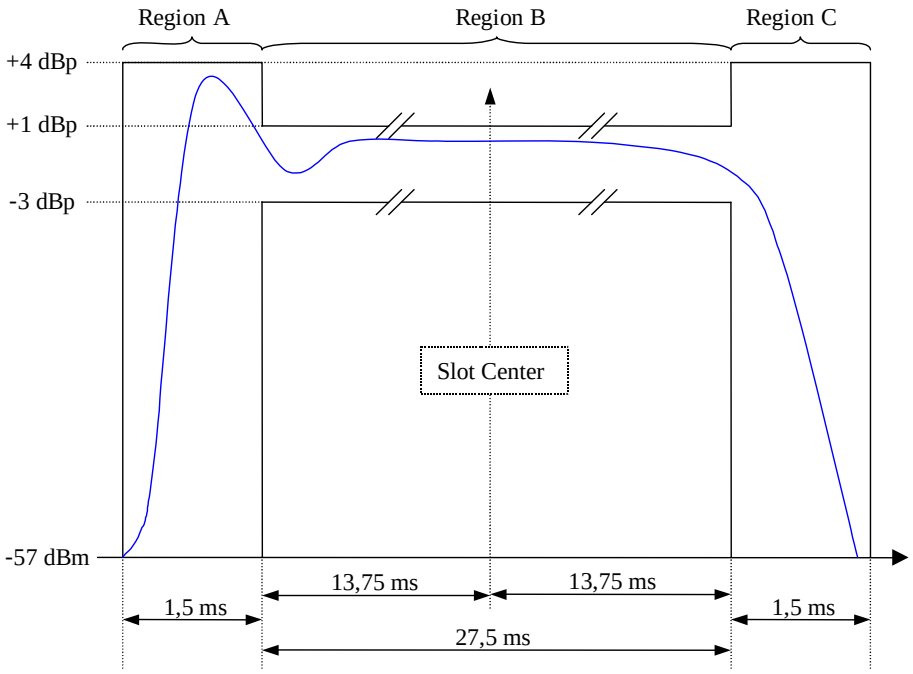


Figure 10.3: Power waveform mask for normal burst

The power levels given in the mask during the 27,5 ms symbol transmission period are given in dBp, where 0 dBp is defined as:

$$0dB_p \equiv \frac{1}{27,5}\int_{-13,75}^{13,75} TxP(t)dt \qquad (3)$$

where:

- $TxP(t)$ is the instantaneous transmitter power; and
- the timing is relative to the slot centre.

Thus, 0 dBp is the average power during the 27,5 ms symbol transmission period, (Region B in figure 10.3). The average power over the symbol transmission period (0 dBp level) shall use the Carrier Power method of measurement and the tolerance to deviation levels as defined in ETSI EN 300 113-1 [1] or ETSI EN 300 390-1 [3].

10.2.3.1.2 Symbol timing

Figure 10.4 depicts the Normal Burst's timing of the four-level symbols within a 30 ms slot. The normal burst contains 132 symbols with 66 symbols on each side of the slot centre. The centre of the first symbol transmitted is 65,5 symbol times from the slot centre.

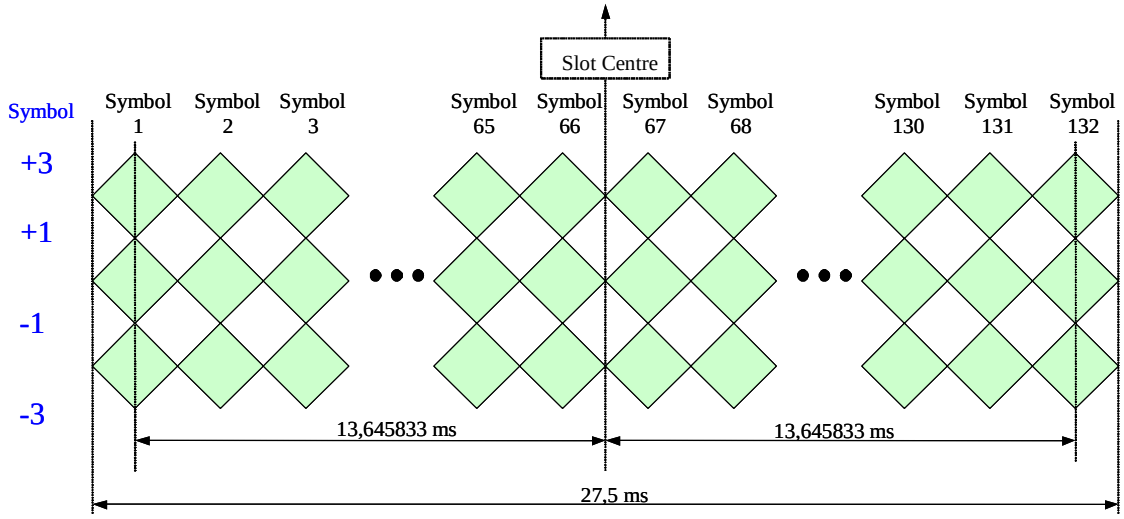


Figure 10.4: Normal burst symbol timing within a slot

10.2.3.1.3 Propagation delay and transmission time

A 1 ms slot timing variation allowance is built in to the Normal Burst structure. This allowance protects against inter-slot interference at the base station receiver caused by:

a) MSs being at different distances from the BS. This results in traffic on the two time-slots being received at very slightly different times at the BS because propagation delay is a function of distance.

b) Each MS having an independent clock with different rates of clock drift resulting in timing differences in signal origination.

Each MS shall time synchronize with the BS before transmitting. Therefore actual time slot timing variation at the beginning of each transmission will result from propagation delay only. Timing differences at the BS may then increase during transmission due to clock drift error.

The total timing deviation from propagation delay and clock drift error combined bounds how far an MS transmitting on the second time slot can be from the BS before inter-slot interference may occur with an MS transmitting on the first time slot in close proximity to the BS. The MSs may, however, resynchronize timing during transmission negating the impact of clock drift error.

In the case where one MS (MS 1) is transmitting on slot 1 in very close proximity to the BS, the 1 ms propagation delay allowance enables another MS (MS 2) to transmit on slot 2 up to 150 km from the BS without inter-slot interference if there is no additional impact of clock drift error. If, however, MS 2 transmits without re-synchronizing during the transmission, time base clock drift error may cause further time deviation from "true" time synchronization and reduce the theoretical range limit below 150 km. Therefore when there is no ongoing clock synchronization it is necessary to make a calculation for both propagation delay and maximum possible clock drift deviation to establish the theoretical distance of the second MS from the base station before inter-slot interference *may* occur. The amount of time in such a calculation for propagation delay is determined by the intended maximum distance of MS 2 from the BS. The amount of variation from clock drift error is determined by call length.

Maximum round trip propagation time is defined by:

Maximum Round Trip Propagation Time = 2 × (Maximum Distance Delta/c)

where:

- c is the speed of light.

NOTE 1: The factor of two is included for round trip propagation delay.

Taking as an example a 135 km maximum distance of MS2 from the base station, 0,9 ms of the 1 ms allowance will needs to be dedicated to propagation delay. This leaves 0,1 ms for time base clock drift during transmission. The maximum time base clock drift error as specified in clause 10.1.4 is ±2 ppm and worse case occurs when one MS clock drifts fast and one MS clock drifts slow. Under this situation, the MS maximum transmission time is defined by:

Maximum Transmission Time = 0,5 × ((Clock Drift Error Allowance) / (Drift per Symbol)) × Symbol Time

where:

- clock drift error allowance is 1 ms - Maximum Round Trip Propagation Time; and
- Drift per Symbol = 0-4 167 ns for 2 ppm clock stability.

NOTE 2: The factor 0,5 is included to take into account drift from two independent MS units drifting in opposite directions in time.

For this 135 km case, where Clock Drift Error Allowance = 0,1 ms, the Maximum Transmission Time is 25 s before inter-slot interference will start to occur in a worst case of clock drift error .

The same calculation can be made for transmitters with better clock drift performance.

For example if the maximum time based error is ±0,5 ppm, MS 2 can be a distance of 146,3 km from the BS and the call will have to exceed 25 s before interference will be experienced in the worst case of clock drift error.

In the case where the MS 1 is also some distance from the BS, the propagation calculations need to take account of the differences in distance between MS 1 and MS 2, not the distance of MS 2 from the BS. The maximum distance in such a case will be limited by a BS unit's sync acquisition window, which is manufacturer specific. For example, where a suitable synch acquisition window exists MS 1 transmitting on slot 1 at a distance of 30 km from the BS enables MS 2 to transmit on slot 2 up to 180 km (150 km + 30 km) km from the BS without inter-slot interference where there is no clock drift error to account for. This may be applicable in deployments when a BS is on a mountain top away from the intended area where radios will be in operational use.

10.2.3.2 Reverse channel (RC) burst

10.2.3.2.0 Reverse channel (RC) burst - Introduction

The RC burst is a short burst that may be used to provide a low data rate channel to a transmitting mobile.

10.2.3.2.1 Power ramp time

The instantaneous transmitter power levels shall be constrained to the mask given in figure 10.5. The mask assures that the power level will be adequate for acceptable BER performance over this very short burst. Inter-slot interference is not an issue here since the burst is so much shorter than the slot time. Since the power level is more tightly constrained than in the Normal Burst, additional ramp time is allocated. Again, 0 dBp is determined by averaging the instantaneous power over Region B of the mask.

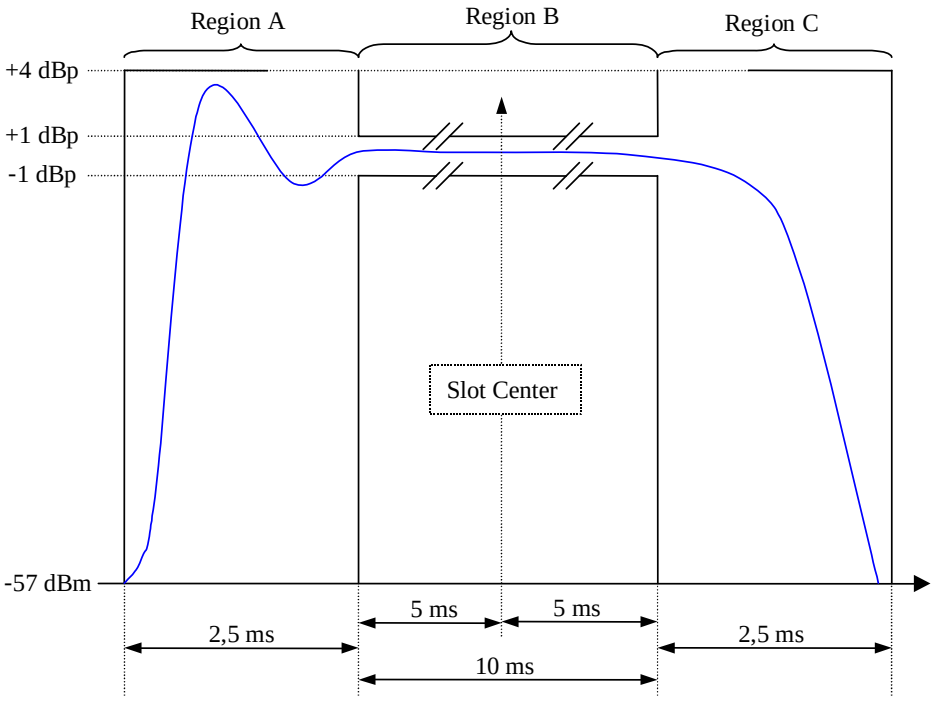


Figure 10.5: Power waveform mask for standalone Reverse Channel (RC) burst

The power levels given in the mask are given during the 10 ms symbol transmission period in dBp, where 0 dBp is defined as:

$$0dB_p \equiv {}^{1}\!/_{10,0} \int_{5,0}^{-5,0} TxP(t)dt \qquad (4)$$

where:

- $TxP(t)$ is the instantaneous transmitter power; and
- the timing is relative to slot centre.

Thus, 0 dBp is the average power during the 10 ms symbol transmission period, (Region B in figure 10.5). The average power over the symbol transmission period (0 dBp level) shall use the Carrier Power method of measurement and the tolerance to deviation levels as defined in ETSI EN 300 113-1 [1] or ETSI EN 300 390-1 [3].

10.2.3.2.2 Symbol timing

Figure 10.6 depicts the RC Burst's timing of the four-level symbols within a 30 ms slot. The normal burst contains 48 symbols with 24 symbols on each side of the slot centre. The centre of the first symbol transmitted is 23,5 symbol times from the slot centre.

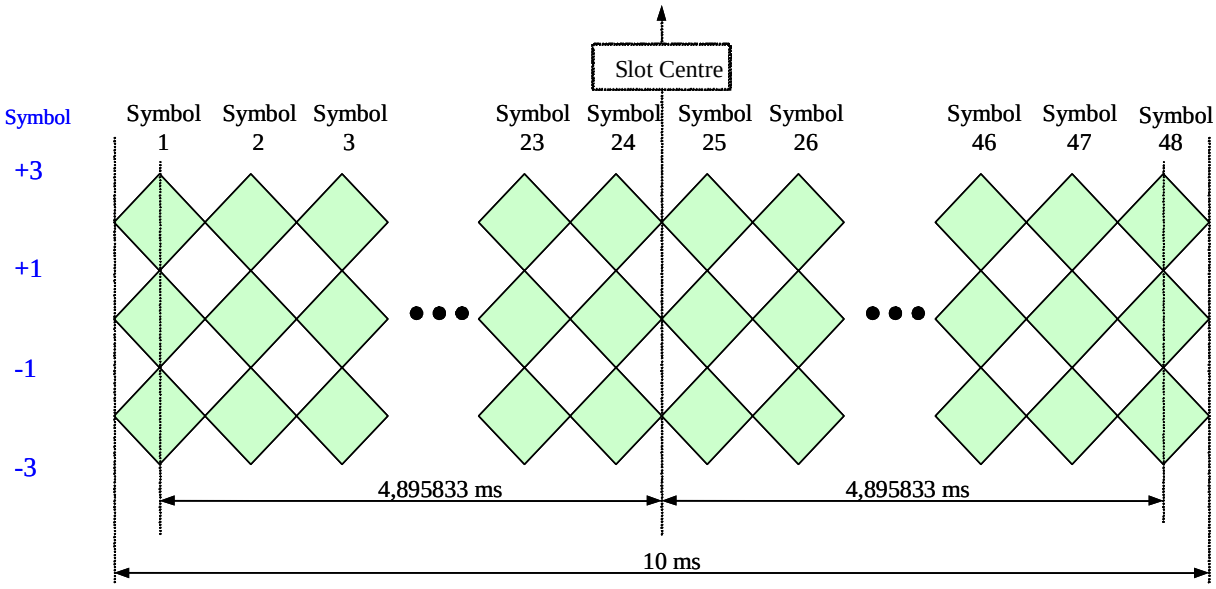


Figure 10.6: Reverse Channel (RC) burst symbol timing within a slot

10.2.3.2.3 Propagation delay

Because the RC Burst is so short, there is no danger of inter-slot interference as there is with the Normal Burst. Still, propagation delay is considered because it affects where the receiver needs to look to find the RC burst. A 1 ms propagation allowance is specified to limit the amount of time the receiver has to spend looking for the RC.

10.2.3.3 Synthesizer Lock-Time constraints

There are different synthesizer lock-time scenarios depending on the type of bursts being sent and received. The synthesizer lock-time specification will be determined by the most restrictive case for which the radio is designed. Direct mode only radios supporting RC signalling shall require a synthesizer lock-time of 11,25 ms. BS mode radios supporting RC signalling shall require a synthesizer lock time of 6,25 ms. In all cases, lock time is defined to be the time required to lock within 100 Hz of the average frequency over the symbol transmission time as defined in clause 10.1.3.

10.2.3.4 Transient frequency constraints during symbol transmission time

To ensure adequate BER performance during the 27,5 ms symbol transmission time, the maximum unmodulated frequency deviation shall be ±100 Hz from the average frequency over the symbol transmission time. The average frequency over the symbol transmission time is defined in clause 10.1.3.

Annex A (normative): Numbering and addressing

All Full Link Control messages shall be used to convey a Source Identifier (ID) which shall identify the individual address of the transmitting entity and a Destination ID which shall identify the address of the receiving entity (or entities). The Source and Destination IDs shall always be 24 bits in length. The DMR addressing scheme is shown in table A.1.

Table A.1: DMR addressing scheme

DMR ID	Name	Number of addresses	Remark
Talkgroup addressing			
000000_{16}	Null	1	Null, see note
000001_{16} - $FFFCDF_{16}$	Talkgroup ID	> 16M	MS talkgroup addresses
$FFFCE0_{16}$ - $FFFFDF_{16}$	Reserved	768	Reserved for future expansion
$FFFFE0_{16}$ - $FFFFEF_{16}$	Unaddressed Idn (n=0-15)	16	Special unaddressed talkgroup IDs
$FFFFF0_{16}$ - $FFFFFF_{16}$	All talkgroup Idn (n=0-15)	16	Special talkgroups containing all MSs
Individual addressing			
000000_{16}	Null	1	Null, see note
000001_{16} - $FFFCDF_{16}$	Unit ID	> 16M	MS individual addresses
$FFFCE0_{16}$ - $FFFEDF_{16}$	Reserved	512	Reserved for future expansion
$FFFEE0_{16}$ - $FFFEEF_{16}$	System gateway Idn (n=0-15)	16	Gateways to system (e.g. repeater) and system interfaced devices not addressable via the DMR ID (e.g. PABX, PSTN, SMS router)
$FFFEF0_{16}$ - $FFFFEF_{16}$	Custom	256	Available for customization
$FFFFF0_{16}$ - $FFFFFF_{16}$	All unit Idn (n=0-15)	16	Special IDs used to address all MSs
NOTE: This is not a valid source or destination address.			

Systems which do not use the partitioned address scheme for "All talkgroup Idn" or "All unit Idn" shall use $FFFFFF_{16}$ to address everybody on the system. In systems with partitioned address schemes, $FFFFF0_{16}$ to $FFFFFF_{16}$ are used to address everybody in each of the respective partitions. Only one scheme shall exist in a particular system.

Annex B (normative): FEC and CRC codes

B.0 FEC and CRC codes - Introduction

Table B.1 summarizes the FEC codes and CRC codes which shall be used in the protocol.

Table B.1: FEC and CRC summary

Field	FEC code	Checksum
EMB field	Quadratic Residue (16,7,6)	none
Slot Type	Golay (20,8)	none
CACH TACT bits	Hamming (7,4)	none
Embedded signalling	Variable length BPTC	5-bit CheckSum (CS)
Reverse Channel (RC) Signalling	RC single burst BPTC	7 bit CRC
Single burst embedded LC	Non-RC single burst BPTC	none
Short LC in CACH	Variable length BPTC	8-bit CRC
PI Header	BPTC(196,96)	CRC-CCITT
Voice LC header	BPTC(196,96)	(12,9) Reed-Solomon
Terminator with LC	BPTC(196,96)	(12,9) Reed-Solomon
CSBK	BPTC(196,96)	CRC-CCITT
Idle message	BPTC(196,96)	none
Data header	BPTC(196,96)	CRC-CCITT
Rate ½ data continuation	BPTC(196,96)	Unconfirmed: none
		Confirmed: CRC-9
Rate ½ last data block	BPTC(196,96)	Unconfirmed: 32-bit CRC
		Confirmed: 32-bit CRC and CRC-9
Rate ¾ data continuation	Rate ¾ Trellis	Unconfirmed: none
		Confirmed: CRC-9
Rate ¾ last data block	Rate ¾ Trellis	Unconfirmed: 32-bit CRC
		Confirmed: 32-bit CRC and CRC-9
Rate 1 non-last data block	Rate 1 coded	Unconfirmed: none
		Confirmed: CRC-9
Rate 1 last data block	Rate 1 coded	Unconfirmed: 32-bit CRC
		Confirmed: 32-bit CRC and CRC-9
Response header block	BPTC(196,96)	CRC-CCITT
Response data block	BPTC(196,96)	32-bit CRC
MBC header	BPTC(196,96)	CRC-CCITT
MBC continuation	BPTC(196,96)	none
MBC last block	BPTC(196,96)	CRC-CCITT
UDT header	BPTC(196,96)	CRC-CCITT
UDT continuation	BPTC(196,96)	none
UDT last block	BPTC(196,96)	CRC-CCITT

The following abbreviations are used in the figures and tables:

AT	Access Type bit
CR	CRC bits
CS	Checksum bit for embedded Full LC
Enc_Dibit	Output Dibit from Trellis Encoder
H	Hamming parity bits
H_Cx	Hamming parity bit from column x of a BPTC
H_Rx	Hamming parity bit from row x of a BPTC
Hx	Hamming parity bit for row X of a BPTC
I	Information bit
LC	Link Control information bit
LCSS	Link Control Start/Stop
P	CACH payload
PC	Parity Check bit
R	Reserved bit
RC	Reverse Channel information bit

TC	TDMA Channel bit
Trellis_Dibit	Output Dibit from Trellis Code
TX	Transmitted bit

B.1 Block Product Turbo Codes

B.1.1 BPTC (196,96)

Control signalling, Unconfirmed and Confirmed data is protected using a (196,96) Block Product Turbo Code illustrated in figure B.1. The 96 bits of information, I(0) - I(95) are placed in a 9 row × 11 column matrix as shown. Three reserved bits, R(0) - R(2), are set to zero and added to round out the payload to 99 bits. Each row is protected using a Hamming (15,11,3) code as indicated with the H_Rx bits. Each column is protected using a Hamming (13,9,3) code as indicated with the H_Cx bits.

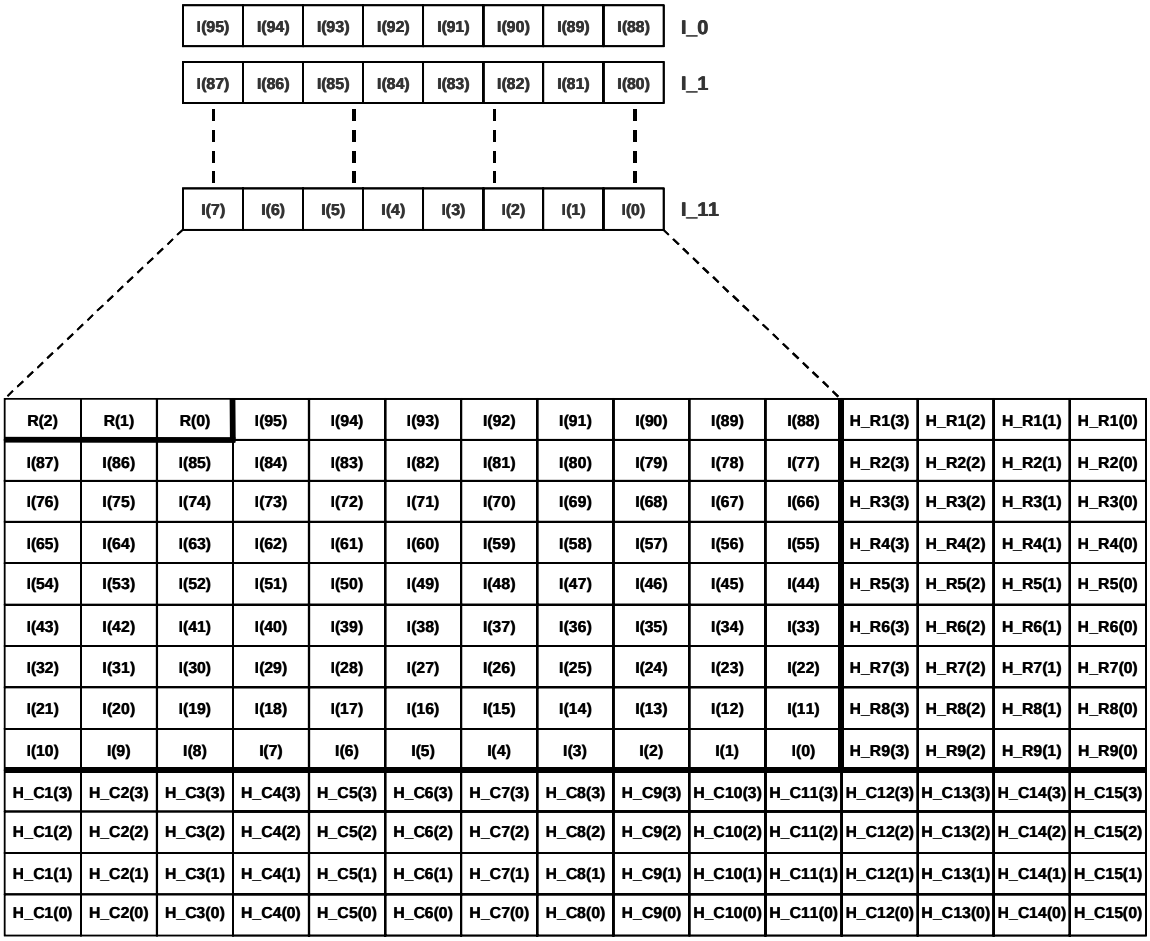


Figure B.1: BPTC (196,96)

The first step in interleaving the bits for the transmission is to sequentially number the bits of the FEC encoded matrix first from left-to-right and then from top to bottom. Table B.2 lists the bits of the Encoder Matrix along with their corresponding indices. In order to pad out the total number of bits to 196, one additional reserved bit, R(3), is set to zero and added to the matrix and assigned index 0. Each bit is then assigned a new index in the interleaved array where:

$$\text{Interleave Index} = \text{Index} \times 181 \text{ modulo } 196$$

The value of the Interleave Index determines the location of each bit in the transmission array, which is placed in the payload of the general data burst.

Table B.3 lists the bit ordering after interleaving. The Index values 0 to 195 correspond to the Interleave Index from the previous table. The resulting array contains 195 bits, numbered from TX(195) down to TX(0) for placement in the payload of the general data burst.

Table B.2: Interleaving indices for BPTC (196,96)

Bit Name	Index	Interleave Index
R(3)	0	0
R(2)	1	181
R(1)	2	166
R(0)	3	151
I(95)	4	136
I(94)	5	121
I(93)	6	106
I(92)	7	91
I(91)	8	76
I(90)	9	61
I(89)	10	46
I(88)	11	31
H_R1(3)	12	16
H_R1(2)	13	1
H_R1(1)	14	182
H_R1(0)	15	167
I(87)	16	152
I(86)	17	137
I(85)	18	122
I(84)	19	107
I(83)	20	92
I(82)	21	77
I(81)	22	62
I(80)	23	47
I(79)	24	32
I(78)	25	17
I(77)	26	2
H_R2(3)	27	183
H_R2(2)	28	168
H_R2(1)	29	153
H_R2(0)	30	138
I(76)	31	123
I(75)	32	108
I(74)	33	93
I(73)	34	78
I(72)	35	63
I(71)	36	48
I(70)	37	33
I(69)	38	18
I(68)	39	3
I(67)	40	184
I(66)	41	169
H_R3(3)	42	154
H_R3(2)	43	139
H_R3(1)	44	124
H_R3(0)	45	109
I(65)	46	94
I(64)	47	79
I(63)	48	64
I(62)	49	49
I(61)	50	34
I(60)	51	19
I(59)	52	4
I(58)	53	185
I(57)	54	170
I(56)	55	155
I(55)	56	140
H_R4(3)	57	125
H_R4(2)	58	110
H_R4(1)	59	95
H_R4(0)	60	80
I(54)	61	65
I(53)	62	50
I(52)	63	35
I(51)	64	20
I(50)	65	5
I(49)	66	186
I(48)	67	171
I(47)	68	156
I(46)	69	141
I(45)	70	126
I(44)	71	111
H_R5(3)	72	96
H_R5(2)	73	81
H_R5(1)	74	66
H_R5(0)	75	51
I(43)	76	36
I(42)	77	21
I(41)	78	6
I(40)	79	187
I(39)	80	172
I(38)	81	157
I(37)	82	142
I(36)	83	127
I(35)	84	112
I(34)	85	97
I(33)	86	82
H_R6(3)	87	67
H_R6(2)	88	52
H_R6(1)	89	37
H_R6(0)	90	22
I(32)	91	7
I(31)	92	188
I(30)	93	173
I(29)	94	158
I(28)	95	143
I(27)	96	128
I(26)	97	113
I(25)	98	98
I(24)	99	83
I(23)	100	68
I(22)	101	53
H_R7(3)	102	38
H_R7(2)	103	23
H_R7(1)	104	8
H_R7(0)	105	189
I(21)	106	174
I(20)	107	159
I(19)	108	144
I(18)	109	129
I(17)	110	114
I(16)	111	99
I(15)	112	84
I(14)	113	69
I(13)	114	54
I(12)	115	39
I(11)	116	24
H_R8(3)	117	9
H_R8(2)	118	190
H_R8(1)	119	175
H_R8(0)	120	160
I(10)	121	145
I(9)	122	130
I(8)	123	115
I(7)	124	100
I(6)	125	85
I(5)	126	70
I(4)	127	55
I(3)	128	40
I(2)	129	25
I(1)	130	10
I(0)	131	191
H_R9(3)	132	176
H_R9(2)	133	161
H_R9(1)	134	146
H_R9(0)	135	131
H_C1(3)	136	116
H_C2(3)	137	101
H_C3(3)	138	86
H_C4(3)	139	71
H_C5(3)	140	56
H_C6(3)	141	41
H_C7(3)	142	26
H_C8(3)	143	11
H_C9(3)	144	192
H_C10(3)	145	177
H_C11(3)	146	162
H_C12(3)	147	147
H_C13(3)	148	132
H_C14(3)	149	117
H_C15(3)	150	102
H_C1(2)	151	87
H_C2(2)	152	72
H_C3(2)	153	57
H_C4(2)	154	42
H_C5(2)	155	27
H_C6(2)	156	12
H_C7(2)	157	193
H_C8(2)	158	178
H_C9(2)	159	163
H_C10(2)	160	148
H_C11(2)	161	133
H_C12(2)	162	118
H_C13(2)	163	103
H_C14(2)	164	88
H_C15(2)	165	73
H_C1(1)	166	58
H_C2(1)	167	43
H_C3(1)	168	28
H_C4(1)	169	13
H_C5(1)	170	194
H_C6(1)	171	179
H_C7(1)	172	164
H_C8(1)	173	149
H_C9(1)	174	134
H_C10(1)	175	119
H_C11(1)	176	104
H_C12(1)	177	89
H_C13(1)	178	74
H_C14(1)	179	59
H_C15(1)	180	44
H_C1(0)	181	29
H_C2(0)	182	14
H_C3(0)	183	195
H_C4(0)	184	180
H_C5(0)	185	165
H_C6(0)	186	150
H_C7(0)	187	135
H_C8(0)	188	120
H_C9(0)	189	105
H_C10(0)	190	90
H_C11(0)	191	75
H_C12(0)	192	60
H_C13(0)	193	45
H_C14(0)	194	30
H_C15(0)	195	15

Table B.3: Transmit bit ordering for BPTC (196,96)

Index	TX Bit	Bit Name
0	TX(195)	R(3)
1	TX(194)	H_R1(2)
2	TX(193)	I(77)
3	TX(192)	I(68)
4	TX(191)	I(59)
5	TX(190)	I(50)
6	TX(189)	I(41)
7	TX(188)	I(32)
8	TX(187)	H_R7(1)
9	TX(186)	H_R8(3)
10	TX(185)	I(1)
11	TX(184)	H_C8(3)
12	TX(183)	H_C6(2)
13	TX(182)	H_C4(1)
14	TX(181)	H_C2(0)
15	TX(180)	H_C15(0)
16	TX(179)	H_R1(3)
17	TX(178)	I(78)
18	TX(177)	I(69)
19	TX(176)	I(60)
20	TX(175)	I(51)
21	TX(174)	I(42)
22	TX(173)	H_R6(0)
23	TX(172)	H_R7(2)
24	TX(171)	I(11)
25	TX(170)	I(2)
26	TX(169)	H_C7(3)
27	TX(168)	H_C5(2)
28	TX(167)	H_C3(1)
29	TX(166)	H_C1(0)
30	TX(165)	H_C14(0)
31	TX(164)	I(88)
32	TX(163)	I(79)
33	TX(162)	I(70)
34	TX(161)	I(61)
35	TX(160)	I(52)
36	TX(159)	I(43)
37	TX(158)	H_R6(1)
38	TX(157)	H_R7(3)
39	TX(156)	I(12)
40	TX(155)	I(3)
41	TX(154)	H_C6(3)
42	TX(153)	H_C4(2)
43	TX(152)	H_C2(1)
44	TX(151)	H_C15(1)
45	TX(150)	H_C13(0)
46	TX(149)	I(89)
47	TX(148)	I(80)
48	TX(147)	I(71)
49	TX(146)	I(62)
50	TX(145)	I(53)
51	TX(144)	H_R5(0)
52	TX(143)	H_R6(2)
53	TX(142)	I(22)
54	TX(141)	I(13)
55	TX(140)	I(4)
56	TX(139)	H_C5(3)
57	TX(138)	H_C3(2)
58	TX(137)	H_C1(1)
59	TX(136)	H_C14(1)
60	TX(135)	H_C12(0)
61	TX(134)	I(90)
62	TX(133)	I(81)
63	TX(132)	I(72)
64	TX(131)	I(63)
65	TX(130)	I(54)
66	TX(129)	H_R5(1)
67	TX(128)	H_R6(3)
68	TX(127)	I(23)
69	TX(126)	I(14)
70	TX(125)	I(5)
71	TX(124)	H_C4(3)
72	TX(123)	H_C2(2)
73	TX(122)	H_C15(2)
74	TX(121)	H_C13(1)
75	TX(120)	H_C11(0)
76	TX(119)	I(91)
77	TX(118)	I(82)
78	TX(117)	I(73)
79	TX(116)	I(64)
80	TX(115)	H_R4(0)
81	TX(114)	H_R5(2)
82	TX(113)	I(33)
83	TX(112)	I(24)
84	TX(111)	I(15)
85	TX(110)	I(6)
86	TX(109)	H_C3(3)
87	TX(108)	H_C1(2)
88	TX(107)	H_C14(2)
89	TX(106)	H_C12(1)
90	TX(105)	H_C10(0)
91	TX(104)	I(92)
92	TX(103)	I(83)
93	TX(102)	I(74)
94	TX(101)	I(65)
95	TX(100)	H_R4(1)
96	TX(99)	H_R5(3)
97	TX(98)	I(34)
98	TX(97)	I(25)
99	TX(96)	I(16)
100	TX(95)	I(7)
101	TX(94)	H_C2(3)
102	TX(93)	H_C15(3)
103	TX(92)	H_C13(2)
104	TX(91)	H_C11(1)
105	TX(90)	H_C9(0)
106	TX(89)	I(93)
107	TX(88)	I(84)
108	TX(87)	I(75)
109	TX(86)	H_R3(0)
110	TX(85)	H_R4(2)
111	TX(84)	I(44)
112	TX(83)	I(35)
113	TX(82)	I(26)
114	TX(81)	I(17)
115	TX(80)	I(8)
116	TX(79)	H_C1(3)
117	TX(78)	H_C14(3)
118	TX(77)	H_C12(2)
119	TX(76)	H_C10(1)
120	TX(75)	H_C8(0)
121	TX(74)	I(94)
122	TX(73)	I(85)
123	TX(72)	I(76)
124	TX(71)	H_R3(1)
125	TX(70)	H_R4(3)
126	TX(69)	I(45)
127	TX(68)	I(36)
128	TX(67)	I(27)
129	TX(66)	I(18)
130	TX(65)	I(9)
131	TX(64)	H_R9(0)
132	TX(63)	H_C13(3)
133	TX(62)	H_C11(2)
134	TX(61)	H_C9(1)
135	TX(60)	H_C7(0)
136	TX(59)	I(95)
137	TX(58)	I(86)
138	TX(57)	H_R2(0)
139	TX(56)	H_R3(2)
140	TX(55)	I(55)
141	TX(54)	I(46)
142	TX(53)	I(37)
143	TX(52)	I(28)
144	TX(51)	I(19)
145	TX(50)	I(10)
146	TX(49)	H_R9(1)
147	TX(48)	H_C12(3)
148	TX(47)	H_C10(2)
149	TX(46)	H_C8(1)
150	TX(45)	H_C6(0)
151	TX(44)	R(0)
152	TX(43)	I(87)
153	TX(42)	H_R2(1)
154	TX(41)	H_R3(3)
155	TX(40)	I(56)
156	TX(39)	I(47)
157	TX(38)	I(38)
158	TX(37)	I(29)
159	TX(36)	I(20)
160	TX(35)	H_R8(0)
161	TX(34)	H_R9(2)
162	TX(33)	H_C11(3)
163	TX(32)	H_C9(2)
164	TX(31)	H_C7(1)
165	TX(30)	H_C5(0)
166	TX(29)	R(1)
167	TX(28)	H_R1(0)
168	TX(27)	H_R2(2)
169	TX(26)	I(66)
170	TX(25)	I(57)
171	TX(24)	I(48)
172	TX(23)	I(39)
173	TX(22)	I(30)
174	TX(21)	I(21)
175	TX(20)	H_R8(1)
176	TX(19)	H_R9(3)
177	TX(18)	H_C10(3)
178	TX(17)	H_C8(2)
179	TX(16)	H_C6(1)
180	TX(15)	H_C4(0)
181	TX(14)	R(2)
182	TX(13)	H_R1(1)
183	TX(12)	H_R2(3)
184	TX(11)	I(67)
185	TX(10)	I(58)
186	TX(9)	I(49)
187	TX(8)	I(40)
188	TX(7)	I(31)
189	TX(6)	H_R7(0)
190	TX(5)	H_R8(2)
191	TX(4)	I(0)
192	TX(3)	H_C9(3)
193	TX(2)	H_C7(2)
194	TX(1)	H_C5(1)
195	TX(0)	H_C3(0)

B.2 Variable length BPTC

B.2.1 Variable length BPTC for embedded signalling

The embedded signalling is protected using a BPTC consisting of Hamming (16,11,4) row codes and simple parity checks for the column codes as illustrated in figure B.2. As the message size increases, additional rows are added to the code, allowing the decoder and parser to keep its basic format for all message lengths. If required, pad bits or error detecting checksums are added to the information in order to round out the length to a multiple of 11 bits.

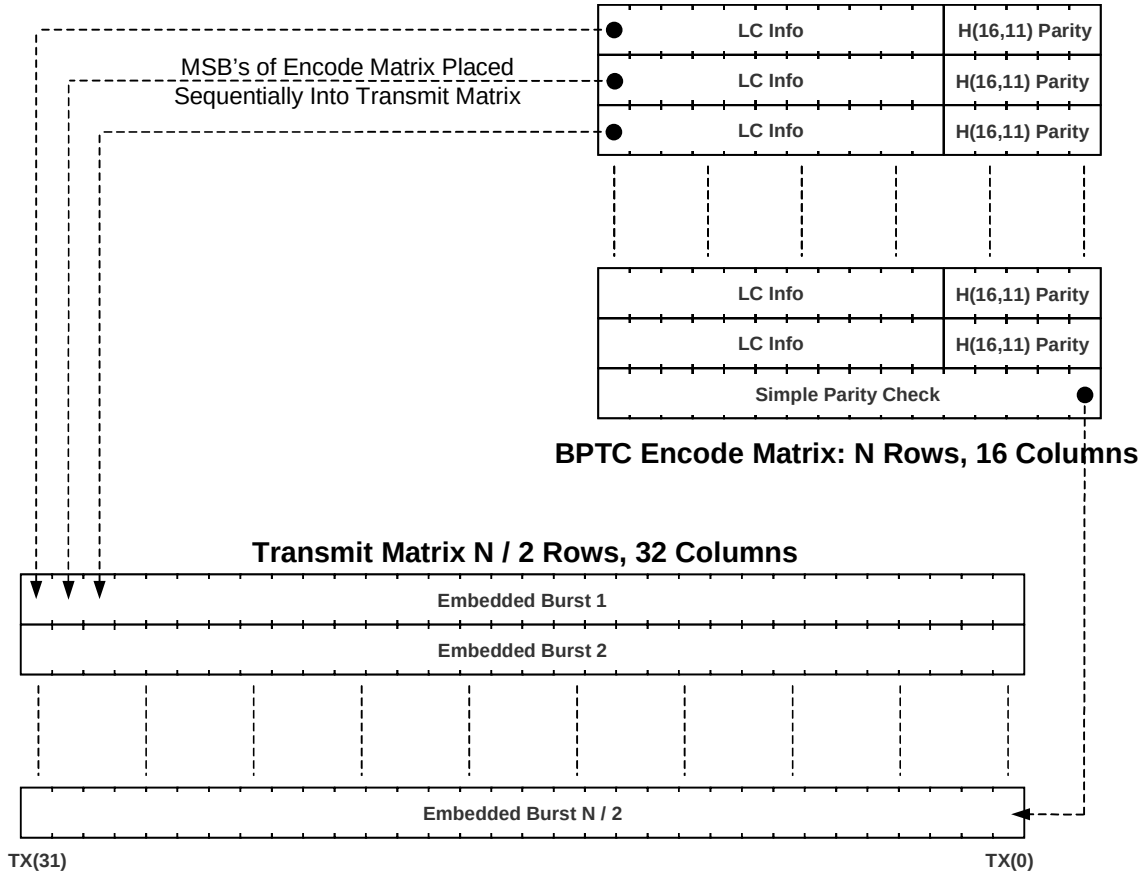


Figure B.2: Format for embedded signalling BPTC

The interleaving schedule for the embedded signalling is also shown in figure B.2. The signalling information, Hamming parity bits, and parity check bits are represented in their FEC encoded form as the BPTC Encode Matrix. The bits are interleaved for transmission by reading the columns of the encoded matrix top-to-bottom and left-to-right and writing the bits into the Transmit Matrix rows left-to-right. Each row of the resulting Transmit Matrix is 32 bits long and is placed in the embedded signalling field of sequential bursts.

Figure B.3 illustrates the burst format used for embedded signalling. The 9 bytes of LC information, LC(71) - LC(0), are placed in the matrix as shown. Each row is protected by its own Hamming code, H1 - H7. The bottom row contains a parity check bit for each column.

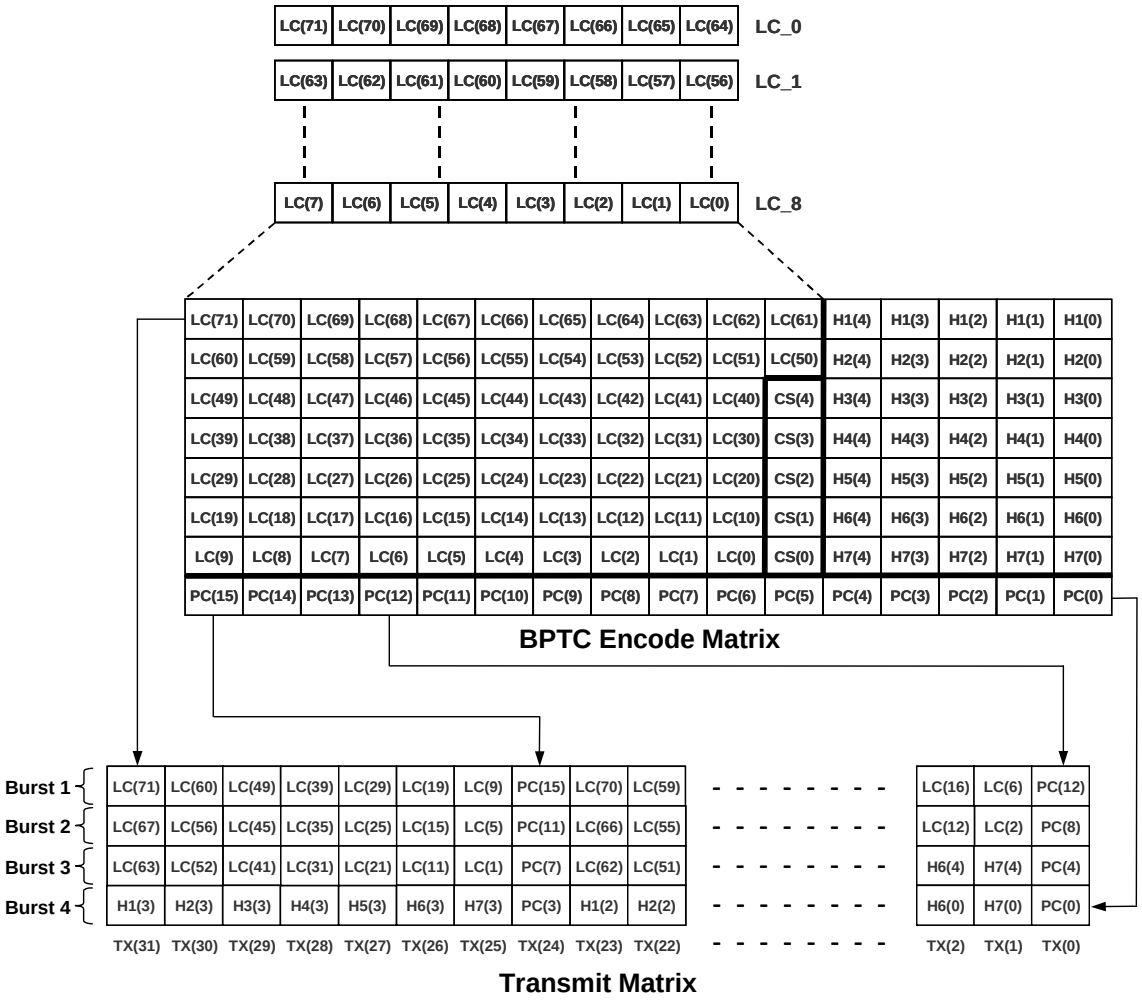


Figure B.3: Format for burst embedded signalling

The calculation of the 5-bit Checksum (CS) is defined in clause B.3.11.

The interleaving schedule for the encoded LC message is shown in figure B.3. The LC signalling information (LC), CheckSum (CS), Hamming parity bits (Hx), and Parity Check bits (PC) are represented in their FEC encoded form as the BPTC Encode Matrix. The parity check bits (PC) shall be chosen such that each column of the BPTC matrix has an even number of "one" bits. Each of the four rows of the resulting Transmit Matrix is placed in sequential bursts according to the definition of the voice superframe.

B.2.2 Single Burst Variable length BPTC

B.2.2.1 Non-Reverse Channel Single Burst BPTC

The non-RC Single Burst FEC is a special case of the embedded signalling code. The format for the BPTC Encode Matrix is the same as for the variable length embedded signalling. However, the interleaving is performed differently to provide additional resistance to errors over a single burst. Figure B.4 illustrates the encoding details for non-RC Single Burst signalling. The 11 bits of non-RC Single Burst signalling, SB(10) - SB(0) are placed in the first row of the matrix and protected with a Hamming (16,11,4) code. The bottom row contains an even parity check bit for each column. In this case, the parity check row is identical to the information row.

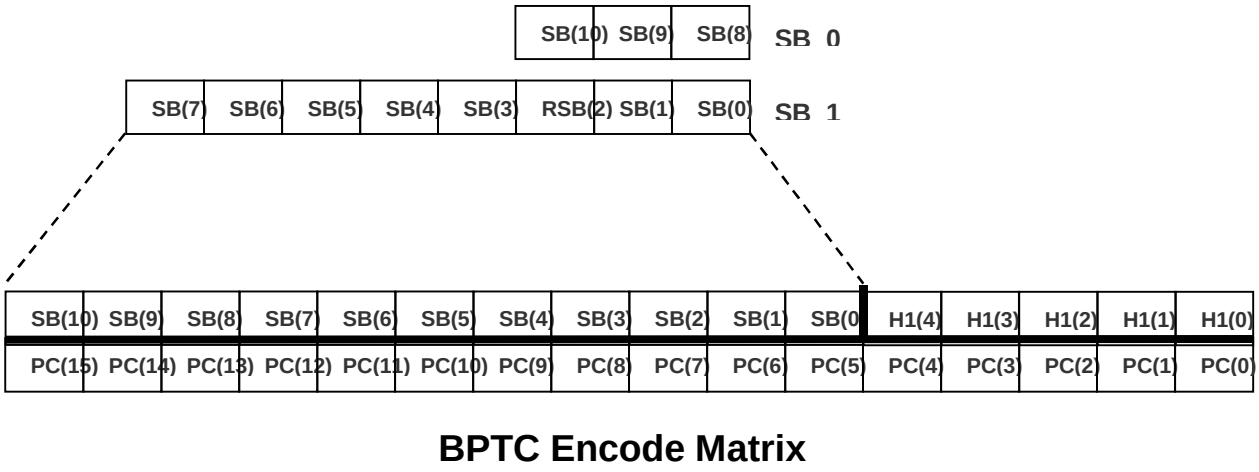


Figure B.4: Format for non-Reverse Channel Single Burst

The first step in interleaving the bits for the transmission is to sequentially number the bits of the FEC encoded matrix from top-to-bottom, left-to-right. Table B.4 lists the bits of the Encoder Matrix along with their corresponding indices. Each bit is then assigned a new index in the interleaved array where:

$$\text{Interleave Index} = \text{Index} \times 17 \text{ modulo } 32.$$

The value of the Interleave Index determines the location of each bit in the transmission array, which is placed in the embedded field.

Table B.4: Interleaving indices for non-Reverse Channel Single Burst

Bit	Index	Interleave Index
SB(10)	0	0
PC(15)	1	17
SB(9)	2	2
PC(14)	3	19
SB(8)	4	4
PC(13)	5	21
SB(7)	6	6
PC(12)	7	23
SB(6)	8	8
PC(11)	9	25
SB(5)	10	10

Bit	Index	Interleave Index
PC(10)	11	27
SB(4)	12	12
PC(9)	13	29
SB(3)	14	14
PC(8)	15	31
SB(2)	16	16
PC(7)	17	1
SB(1)	18	18
PC(6)	19	3
SB(0)	20	20
PC(5)	21	5

Bit	Index	Interleave Index
H(4)	22	22
PC(4)	23	7
H(3)	24	24
PC(3)	25	9
H(2)	26	26
PC(2)	27	11
H(1)	28	28
PC(1)	29	13
H(0)	30	30
PC(0)	31	15

Table B.5 lists the bit ordering after interleaving. The index values 0 to 31 correspond to the Interleave Index from the previous table. The resulting array contains 32 bits, numbered from TX(31) down to TX(0) for placement in the embedded field.

Table B.5: Transmit bit ordering for non-Reverse Channel Single Burst

Index	Bit	TX Bit
0	SB(10)	TX(31)
1	PC(7)	TX(30)
2	SB(9)	TX(29)
3	PC(6)	TX(28)
4	SB(8)	TX(27)
5	PC(5)	TX(26)
6	SB(7)	TX(25)
7	PC(4)	TX(24)
8	SB(6)	TX(23)
9	PC(3)	TX(22)
10	SB(5)	TX(21)

Index	Bit	TX Bit
11	PC(2)	TX(20)
12	SB(4)	TX(19)
13	PC(1)	TX(18)
14	SB(3)	TX(17)
15	PC(0)	TX(16)
16	SB(2)	TX(15)
17	PC(15)	TX(14)
18	SB(1)	TX(13)
19	PC(14)	TX(12)
20	SB(0)	TX(11)
21	PC(13)	TX(10)

Index	Bit	TX Bit
22	H(4)	TX(9)
23	PC(12)	TX(8)
24	H(3)	TX(7)
25	PC(11)	TX(6)
26	H(2)	TX(5)
27	PC(10)	TX(4)
28	H(1)	TX(3)
29	PC(9)	TX(2)
30	H(0)	TX(1)
31	PC(8)	TX(0)

B.2.2.2 Reverse Channel Single Burst BPTC

The RC Single Burst FEC is a special case of the embedded signalling code. The format for the BPTC Encode Matrix is the same as for the variable length embedded signalling. However, the interleaving is performed differently to provide additional resistance to errors over a single burst. Figure B.4A illustrates the encoding details for RC signalling. The 11 bits of RC signalling, RC(10) - RC(0) are placed in the first row of the matrix and protected with a Hamming (16,11,4) code. The bottom row contains an odd parity check bit for each column. In this case, the parity check row is opposite to the information row.

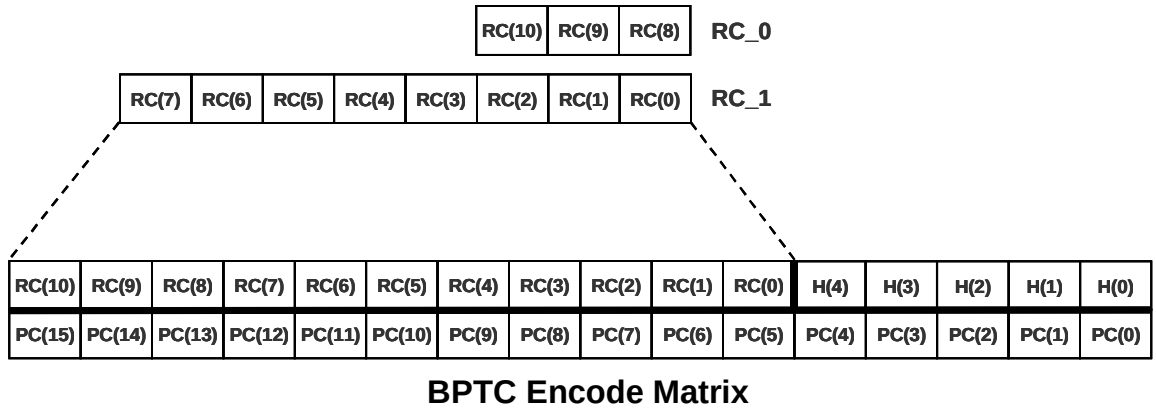


Figure B.4A: Format for Reverse Channel

The first step in interleaving the bits for the transmission is to sequentially number the bits of the FEC encoded matrix from top-to-bottom, left-to-right. Table B.4A lists the bits of the Encoder Matrix along with their corresponding indices. Each bit is then assigned a new index in the interleaved array where:

$$\text{Interleave Index} = \text{Index} \times 17 \text{ modulo } 32.$$

The value of the Interleave Index determines the location of each bit in the transmission array, which is placed in the embedded field.

Table B.4A: Interleaving indices for Reverse Channel

Bit	Index	Interleave Index
RC(10)	0	0
PC(15)	1	17
RC(9)	2	2
PC(14)	3	19
RC(8)	4	4
PC(13)	5	21
RC(7)	6	6
PC(12)	7	23
RC(6)	8	8
PC(11)	9	25
RC(5)	10	10

Bit	Index	Interleave Index
PC(10)	11	27
RC(4)	12	12
PC(9)	13	29
RC(3)	14	14
PC(8)	15	31
RC(2)	16	16
PC(7)	17	1
RC(1)	18	18
PC(6)	19	3
RC(0)	20	20
PC(5)	21	5

Bit	Index	Interleave Index
H(4)	22	22
PC(4)	23	7
H(3)	24	24
PC(3)	25	9
H(2)	26	26
PC(2)	27	11
H(1)	28	28
PC(1)	29	13
H(0)	30	30
PC(0)	31	15

Table B.5A lists the bit ordering after interleaving. The index values 0 to 31 correspond to the Interleave Index from the previous table. The resulting array contains 32 bits, numbered from TX(31) down to TX(0) for placement in the embedded field.

Table B.5A: Transmit bit ordering for Reverse Channel

Index	Bit	TX Bit
0	RC(10)	TX(31)
1	PC(7)	TX(30)
2	RC(9)	TX(29)
3	PC(6)	TX(28)
4	RC(8)	TX(27)
5	PC(5)	TX(26)
6	RC(7)	TX(25)
7	PC(4)	TX(24)
8	RC(6)	TX(23)
9	PC(3)	TX(22)
10	RC(5)	TX(21)

Index	Bit	TX Bit
11	PC(2)	TX(20)
12	RC(4)	TX(19)
13	PC(1)	TX(18)
14	RC(3)	TX(17)
15	PC(0)	TX(16)
16	RC(2)	TX(15)
17	PC(15)	TX(14)
18	RC(1)	TX(13)
19	PC(14)	TX(12)
20	RC(0)	TX(11)
21	PC(13)	TX(10)

Index	Bit	TX Bit
22	H(4)	TX(9)
23	PC(12)	TX(8)
24	H(3)	TX(7)
25	PC(11)	TX(6)
26	H(2)	TX(5)
27	PC(10)	TX(4)
28	H(1)	TX(3)
29	PC(9)	TX(2)
30	H(0)	TX(1)
31	PC(8)	TX(0)

B.2.3 Variable length BPTC for CACH signalling

The CACH signalling is protected using a BPTC consisting of Hamming (17,12,3) row codes and simple parity checks for the column codes as illustrated in figure B.5. As the message size increases, additional rows are added to the code. If required, pad bits or error detecting checksums are added to the information in order to round out the length to a multiple of 12 bits.

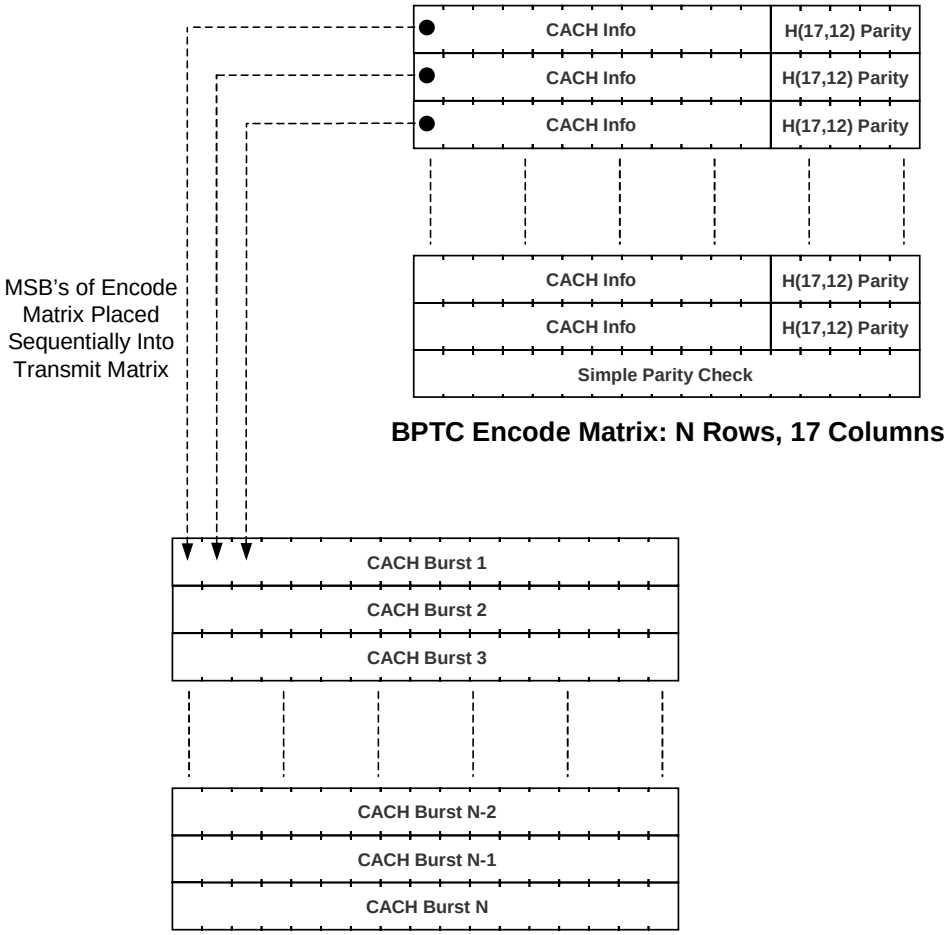


Figure B.5: Format for CACH BPTC

The interleaving schedule for the CACH signalling is also shown in figure B.5. The signalling information, Hamming parity bits, and simple parity check bits are represented in their FEC encoded form as the BPTC Encode Matrix. The bits are interleaved for transition by reading the columns of the encoded matrix top-to-bottom and left-to-right and writing the bits into the Transmit Matrix rows left-to-right. Each row of the resulting Transmit Matrix has a length of 17 bits and is placed in the payload field of sequential CACH bursts.

Figure B.6 illustrates the specifics of encoding Short LC messages for transmission in the CACH. The 3 ½ octets of LC information, LC(27) - LC(0), are placed in the matrix as shown. A 1-byte CRC, CR(7) - CR(0), is also added. This CRC is defined in clause B.3.7.

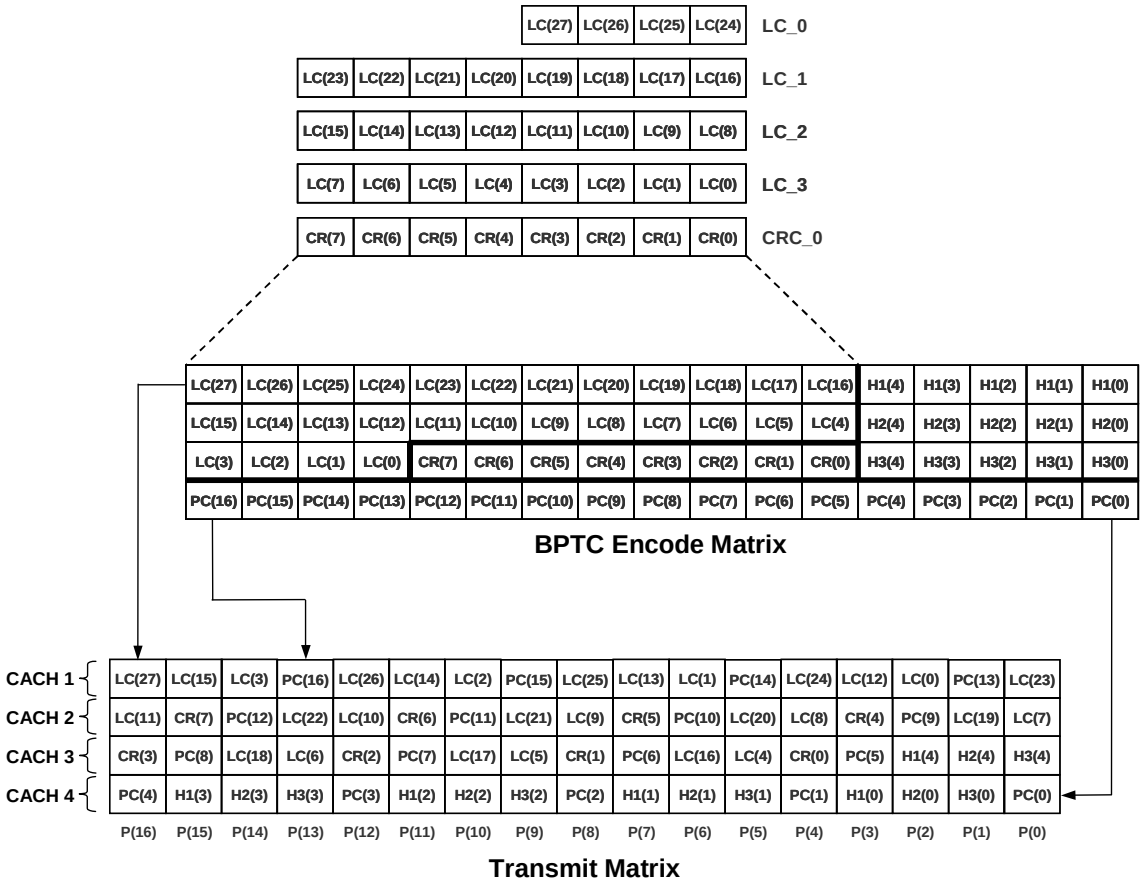


Figure B.6: Format for Short LC in CACH

The interleaving schedule for the 4-burst CACH message is also shown in figure B.6. The signalling information (LC), Hamming parity bits (Hx), and parity check bits (PC) are represented in their FEC encoded form as the BPTC Encode Matrix. The parity check bits (PC) shall be chosen such that each column of the BPTC matrix has an even number of "one" bits. Each of the four rows of the Transmit Matrix is placed in sequential CACH bursts.

For the Short LC messages an 8-bit CRC shall be used as described in clause B.3.7.

B.2.4 Rate ¾ Trellis code

The data blocks for Unconfirmed and Confirmed data packets use a rate ¾ trellis code. The encoding process of the rate ¾ code is diagrammed in figure B.7.

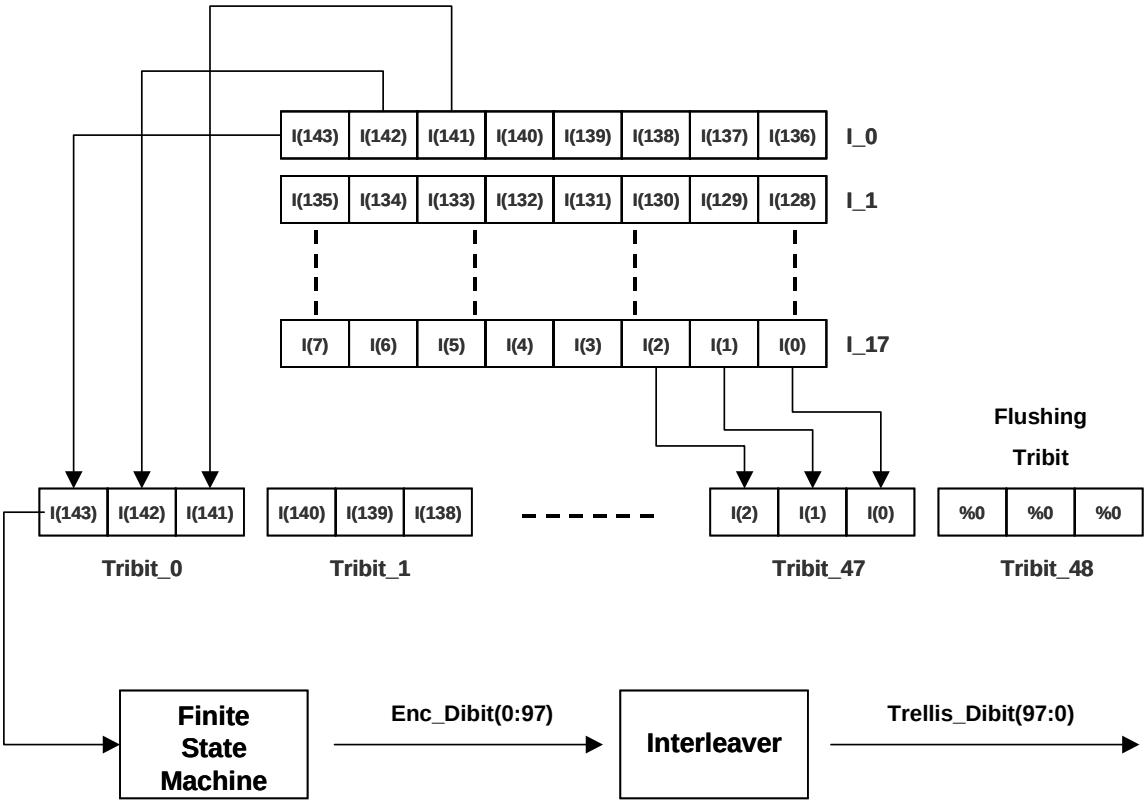


Figure B.7: Rate ¾ Trellis encoder overview

The encoding process begins by serializing a sequence of octets as shown, from left to right, and then separating the result into a serial stream of tribits. Each tribit contains three bits with the most significant bit to the left and the least significant bit to the right. Consequently, each tribit is represented by an octal number in the range 0 to 7. The tribit stream is applied to the trellis encoder, starting with tribit 0 and ending with tribit m-1.

Table B.6: Trellis code word sizes

	Rate ¾
Input Size	48 tribits
Output Size	98 dibits
(n,k)	(196,144)

The Trellis encoder is implemented as a finite state machine, or FSM. It appends a 000_2 tribit at the end of the stream to flush out the final state. The dibits on the output are mapped to ±1, ±3 amplitudes and then interleaved before being modulated.

The Trellis encoder receives m tribits as input, and outputs 2m dibits. The encoding process is diagrammed below in figure B.8. The encoder is an 8-state Finite State Machine (FSM) for the code rate ¾, with an initial state of zero. The FSM used in this particular implementation has the special property of having the current input as the next state. For each tribit input, there is a corresponding output constellation point which is represented as a dibit pair.

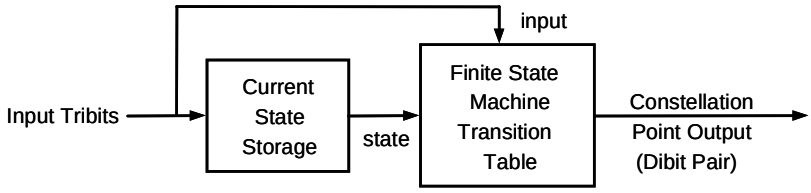


Figure B.8: Trellis encoder block diagram

The state transition is shown in table B.7. The output of the state transition table is one of 16 constellation points. The constellation to dibit pair mapping is shown in table B.8.

Table B.7: Trellis encoder state transition table

		Input Tribit							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
	0	0	8	4	12	2	10	6	14
	1	4	12	2	10	6	14	0	8
	2	1	9	5	13	3	11	7	15
FSM	**3**	5	13	3	11	7	15	1	9
State	**4**	3	11	7	15	1	9	5	13
	5	7	15	1	9	5	13	3	11
	6	2	10	6	14	0	8	4	12
	7	6	14	0	8	4	12	2	10

Table B.8: Constellation to dibit pair mapping

Constellation Point	Dibit 0	Dibit 1	Constellation Point	Dibit 0	Dibit 1
0	+1	-1	8	-3	+3
1	-1	-1	9	+3	+3
2	+3	-3	10	-1	+1
3	-3	-3	11	+1	+1
4	-3	-1	12	+1	+3
5	+3	-1	13	-1	+3
6	-1	-3	14	+3	+1
7	+1	-3	15	-3	+1

Interleaving is done for data blocks for the code rate ¾. The purpose of the interleaver is to spread burst errors due to Rayleigh fading over the 98 dibit block. In the interleaver, the dibit array is rearranged to form another dibit array according to the interleave table shown in table B.9.

Table B.9: Interleaving schedule for rate ¾ Trellis code

Interleave Table							
Enc Index	**Input Index**	**Enc Index**	**Input Index**	**Enc Index**	**Input Index**	**Enc Index**	**Input Index**
0	0	26	2	50	4	74	6
1	1	27	3	51	5	75	7
2	8	28	10	52	12	76	14
3	9	29	11	53	13	77	15
4	16	30	18	54	20	78	22
5	17	31	19	55	21	79	23
6	24	32	26	56	28	80	30
7	25	33	27	57	29	81	31
8	32	34	34	58	36	82	38
9	33	35	35	59	37	83	39
10	40	36	42	60	44	84	46
11	41	37	43	61	45	85	47
12	48	38	50	62	52	86	54
13	49	39	51	63	53	87	55
14	56	40	58	64	60	88	62
15	57	41	59	65	61	89	63
16	64	42	66	66	68	90	70
17	65	43	67	67	69	91	71
18	72	44	74	68	76	92	78
19	73	45	75	69	77	93	79
20	80	46	82	70	84	94	86
21	81	47	83	71	85	95	87
22	88	48	90	72	92	96	94
23	89	49	91	73	93	97	95
24	96						
25	97						

Table B.10 provides the transmit bit order based on the interleaving schedule. The 98 Trellis Dibits that are placed in the general data burst for transmission are listed out along with the corresponding dibits that are output from the encoder.

Table B.10: Transmit bit ordering for rate ¾ Trellis code

Index	TX Dibit	Dibit
0	Trellis_Dibit(97)	Enc_Dibit(0)
1	Trellis_Dibit(96)	Enc_Dibit(1)
2	Trellis_Dibit(95)	Enc_Dibit(8)
3	Trellis_Dibit(94)	Enc_Dibit(9)
4	Trellis_Dibit(93)	Enc_Dibit(16)
5	Trellis_Dibit(92)	Enc_Dibit(17)
6	Trellis_Dibit(91)	Enc_Dibit(24)
7	Trellis_Dibit(90)	Enc_Dibit(25)
8	Trellis_Dibit(89)	Enc_Dibit(32)
9	Trellis_Dibit(88)	Enc_Dibit(33)
10	Trellis_Dibit(87)	Enc_Dibit(40)
11	Trellis_Dibit(86)	Enc_Dibit(41)
12	Trellis_Dibit(85)	Enc_Dibit(48)
13	Trellis_Dibit(84)	Enc_Dibit(49)
14	Trellis_Dibit(83)	Enc_Dibit(56)
15	Trellis_Dibit(82)	Enc_Dibit(57)
16	Trellis_Dibit(81)	Enc_Dibit(64)
17	Trellis_Dibit(80)	Enc_Dibit(65)
18	Trellis_Dibit(79)	Enc_Dibit(72)
19	Trellis_Dibit(78)	Enc_Dibit(73)
20	Trellis_Dibit(77)	Enc_Dibit(80)
21	Trellis_Dibit(76)	Enc_Dibit(81)
22	Trellis_Dibit(75)	Enc_Dibit(88)
23	Trellis_Dibit(74)	Enc_Dibit(89)
24	Trellis_Dibit(73)	Enc_Dibit(96)
25	Trellis_Dibit(72)	Enc_Dibit(97)
26	Trellis_Dibit(71)	Enc_Dibit(2)
27	Trellis_Dibit(70)	Enc_Dibit(3)
28	Trellis_Dibit(69)	Enc_Dibit(10)
29	Trellis_Dibit(68)	Enc_Dibit(11)
30	Trellis_Dibit(67)	Enc_Dibit(18)
31	Trellis_Dibit(66)	Enc_Dibit(19)
32	Trellis_Dibit(65)	Enc_Dibit(26)
33	Trellis_Dibit(64)	Enc_Dibit(27)
34	Trellis_Dibit(63)	Enc_Dibit(34)
35	Trellis_Dibit(62)	Enc_Dibit(35)
36	Trellis_Dibit(61)	Enc_Dibit(42)
37	Trellis_Dibit(60)	Enc_Dibit(43)
38	Trellis_Dibit(59)	Enc_Dibit(50)
39	Trellis_Dibit(58)	Enc_Dibit(51)
40	Trellis_Dibit(57)	Enc_Dibit(58)
41	Trellis_Dibit(56)	Enc_Dibit(59)
42	Trellis_Dibit(55)	Enc_Dibit(66)
43	Trellis_Dibit(54)	Enc_Dibit(67)
44	Trellis_Dibit(53)	Enc_Dibit(74)
45	Trellis_Dibit(52)	Enc_Dibit(75)
46	Trellis_Dibit(51)	Enc_Dibit(82)
47	Trellis_Dibit(50)	Enc_Dibit(83)
48	Trellis_Dibit(49)	Enc_Dibit(90)

Index	TX Dibit	Dibit
49	Trellis_Dibit(48)	Enc_Dibit(91)
50	Trellis_Dibit(47)	Enc_Dibit(4)
51	Trellis_Dibit(46)	Enc_Dibit(5)
52	Trellis_Dibit(45)	Enc_Dibit(12)
53	Trellis_Dibit(44)	Enc_Dibit(13)
54	Trellis_Dibit(43)	Enc_Dibit(20)
55	Trellis_Dibit(42)	Enc_Dibit(21)
56	Trellis_Dibit(41)	Enc_Dibit(28)
57	Trellis_Dibit(40)	Enc_Dibit(29)
58	Trellis_Dibit(39)	Enc_Dibit(36)
59	Trellis_Dibit(38)	Enc_Dibit(37)
60	Trellis_Dibit(37)	Enc_Dibit(44)
61	Trellis_Dibit(36)	Enc_Dibit(45)
62	Trellis_Dibit(35)	Enc_Dibit(52)
63	Trellis_Dibit(34)	Enc_Dibit(53)
64	Trellis_Dibit(33)	Enc_Dibit(60)
65	Trellis_Dibit(32)	Enc_Dibit(61)
66	Trellis_Dibit(31)	Enc_Dibit(68)
67	Trellis_Dibit(30)	Enc_Dibit(69)
68	Trellis_Dibit(29)	Enc_Dibit(76)
69	Trellis_Dibit(28)	Enc_Dibit(77)
70	Trellis_Dibit(27)	Enc_Dibit(84)
71	Trellis_Dibit(26)	Enc_Dibit(85)
72	Trellis_Dibit(25)	Enc_Dibit(92)
73	Trellis_Dibit(24)	Enc_Dibit(93)
74	Trellis_Dibit(23)	Enc_Dibit(6)
75	Trellis_Dibit(22)	Enc_Dibit(7)
76	Trellis_Dibit(21)	Enc_Dibit(14)
77	Trellis_Dibit(20)	Enc_Dibit(15)
78	Trellis_Dibit(19)	Enc_Dibit(22)
79	Trellis_Dibit(18)	Enc_Dibit(23)
80	Trellis_Dibit(17)	Enc_Dibit(30)
81	Trellis_Dibit(16)	Enc_Dibit(31)
82	Trellis_Dibit(15)	Enc_Dibit(38)
83	Trellis_Dibit(14)	Enc_Dibit(39)
84	Trellis_Dibit(13)	Enc_Dibit(46)
85	Trellis_Dibit(12)	Enc_Dibit(47)
86	Trellis_Dibit(11)	Enc_Dibit(54)
87	Trellis_Dibit(10)	Enc_Dibit(55)
88	Trellis_Dibit(9)	Enc_Dibit(62)
89	Trellis_Dibit(8)	Enc_Dibit(63)
90	Trellis_Dibit(7)	Enc_Dibit(70)
91	Trellis_Dibit(6)	Enc_Dibit(71)
92	Trellis_Dibit(5)	Enc_Dibit(78)
93	Trellis_Dibit(4)	Enc_Dibit(79)
94	Trellis_Dibit(3)	Enc_Dibit(86)
95	Trellis_Dibit(2)	Enc_Dibit(87)
96	Trellis_Dibit(1)	Enc_Dibit(94)
97	Trellis_Dibit(0)	Enc_Dibit(95)

B.2.5 Rate 1 coded data

Rate 1 coding is used to transmit data blocks for Confirmed or Unconfirmed data packets as described in clauses 8.2.2.1 and 8.2.2.2. No encoding rules apply to the payload as shown in figure B.8A.

A simple encoding algorithm is done for data blocks for the code rate 1. The main purpose of this algorithm is to adapt the 192 payload bit to the 196 packet size bits. The algorithm is shown in table B.10B that illustrates the transmit bit order for the data bits.

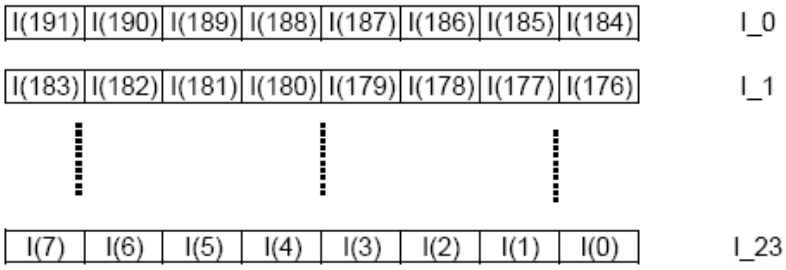


Figure B.8A: Rate 1 user data

To reach the 196 bits length from 192 used data four padding bits shall be added. These four bits are all set to zero as shown in table B.10A.

Table B.10A: Padding bits for rate 1 coded data

Pad bit	Value
P(0)	0
P(1)	0
P(2)	0
P(3)	0

The transmit bit order using information bits and padding bits is illustrated in table B.10B.

Table B.10B: Transmit bit ordering for rate 1 coded data

Index	TX Bit	Bit Name
0	TX(195)	I(191)
1	TX(194)	I(190)
2	TX(193)	I(189)
3	TX(192)	I(188)
4	TX(191)	I(187)
5	TX(190)	I(186)
6	TX(189)	I(185)
7	TX(188)	I(184)
8	TX(187)	I(183)
9	TX(186)	I(182)
10	TX(185)	I(181)
11	TX(184)	I(180)
12	TX(183)	I(179)
13	TX(182)	I(178)
14	TX(181)	I(177)
15	TX(180)	I(176)
16	TX(179)	I(175)
17	TX(178)	I(174)
18	TX(177)	I(173)
19	TX(176)	I(172)
20	TX(175)	I(171)
21	TX(174)	I(170)
22	TX(173)	I(169)
23	TX(172)	I(168)
24	TX(171)	I(167)
25	TX(170)	I(166)
26	TX(169)	I(165)
27	TX(168)	I(164)
28	TX(167)	I(163)
29	TX(166)	I(162)
30	TX(165)	I(161)
31	TX(164)	I(160)
32	TX(163)	I(159)
33	TX(162)	I(158)
34	TX(161)	I(157)
35	TX(160)	I(156)
36	TX(159)	I(155)
37	TX(158)	I(154)
38	TX(157)	I(153)
39	TX(156)	I(152)
40	TX(155)	I(151)
41	TX(154)	I(150)
42	TX(153)	I(149)
43	TX(152)	I(148)
44	TX(151)	I(147)
45	TX(150)	I(146)
46	TX(149)	I(145)
47	TX(148)	I(144)
48	TX(147)	I(143)
49	TX(146)	I(142)
50	TX(145)	I(141)
51	TX(144)	I(140)
52	TX(143)	I(139)
53	TX(142)	I(138)
54	TX(141)	I(137)
55	TX(140)	I(136)
56	TX(139)	I(135)
57	TX(138)	I(134)
58	TX(137)	I(133)
59	TX(136)	I(132)
60	TX(135)	I(131)
61	TX(134)	I(130)
62	TX(133)	I(129)
63	TX(132)	I(128)
64	TX(131)	I(127)
65	TX(130)	I(126)
66	TX(129)	I(125)
67	TX(128)	I(124)
68	TX(127)	I(123)
69	TX(126)	I(122)
70	TX(125)	I(121)
71	TX(124)	I(120)
72	TX(123)	I(119)
73	TX(122)	I(118)
74	TX(121)	I(117)
75	TX(120)	I(116)
76	TX(119)	I(115)
77	TX(118)	I(114)
78	TX(117)	I(113)
79	TX(116)	I(112)
80	TX(115)	I(111)
81	TX(114)	I(110)
82	TX(113)	I(109)
83	TX(112)	I(108)
84	TX(111)	I(107)
85	TX(110)	I(106)
86	TX(109)	I(105)
87	TX(108)	I(104)
88	TX(107)	I(103)
89	TX(106)	I(102)
90	TX(105)	I(101)
91	TX(104)	I(100)
92	TX(103)	I(99)
93	TX(102)	I(98)
94	TX(101)	I(97)
95	TX(100)	I(96)
96	TX(99)	P(0)
97	TX(98)	P(1)
98	TX(97)	P(2)
99	TX(96)	P(3)
100	TX(95)	I(95)
101	TX(94)	I(94)
102	TX(93)	I(93)
103	TX(92)	I(92)
104	TX(91)	I(91)
105	TX(90)	I(90)
106	TX(89)	I(89)
107	TX(88)	I(88)
108	TX(87)	I(87)
109	TX(86)	I(86)
110	TX(85)	I(85)
111	TX(84)	I(84)
112	TX(83)	I(83)
113	TX(82)	I(82)
114	TX(81)	I(81)
115	TX(80)	I(80)
116	TX(79)	I(79)
117	TX(78)	I(78)
118	TX(77)	I(77)
119	TX(76)	I(76)
120	TX(75)	I(75)
121	TX(74)	I(74)
122	TX(73)	I(73)
123	TX(72)	I(72)
124	TX(71)	I(71)
125	TX(70)	I(70)
126	TX(69)	I(69)
127	TX(68)	I(68)
128	TX(67)	I(67)
129	TX(66)	I(66)
130	TX(65)	I(65)
131	TX(64)	I(64)
132	TX(63)	I(63)
133	TX(62)	I(62)
134	TX(61)	I(61)
135	TX(60)	I(60)
136	TX(59)	I(59)
137	TX(58)	I(58)
138	TX(57)	I(57)
139	TX(56)	I(56)
140	TX(55)	I(55)
141	TX(54)	I(54)
142	TX(53)	I(53)
143	TX(52)	I(52)
144	TX(51)	I(51)
145	TX(50)	I(50)
146	TX(49)	I(49)
147	TX(48)	I(48)
148	TX(47)	I(47)
149	TX(46)	I(46)
150	TX(45)	I(45)
151	TX(44)	I(44)
152	TX(43)	I(43)
153	TX(42)	I(42)
154	TX(41)	I(41)
155	TX(40)	I(40)
156	TX(39)	I(39)
157	TX(38)	I(38)
158	TX(37)	I(37)
159	TX(36)	I(36)
160	TX(35)	I(35)
161	TX(34)	I(34)
162	TX(33)	I(33)
163	TX(32)	I(32)
164	TX(31)	I(31)
165	TX(30)	I(30)
166	TX(29)	I(29)
167	TX(28)	I(28)
168	TX(27)	I(27)
169	TX(26)	I(26)
170	TX(25)	I(25)
171	TX(24)	I(24)
172	TX(23)	I(23)
173	TX(22)	I(22)
174	TX(21)	I(21)
175	TX(20)	I(20)
176	TX(19)	I(19)
177	TX(18)	I(18)
178	TX(17)	I(17)
179	TX(16)	I(16)
180	TX(15)	I(15)
181	TX(14)	I(14)
182	TX(13)	I(13)
183	TX(12)	I(12)
184	TX(11)	I(11)
185	TX(10)	I(10)
186	TX(9)	I(9)
187	TX(8)	I(8)
188	TX(7)	I(7)
189	TX(6)	I(6)
190	TX(5)	I(5)
191	TX(4)	I(4)
192	TX(3)	I(3)
193	TX(2)	I(2)
194	TX(1)	I(1)
195	TX(0)	I(0)

B.3 Generator matrices and polynomials

B.3.1 Golay (20,8)

The (20,8,7) Golay code is derived by shortening the primitive code generated from the polynomial g(x) given below:

$$g(x) = x^{11} + x^{10} + x^6 + x^5 + x^4 + x^2 + 1 = 6165_8 \quad \text{(B.1)}$$

The generator matrix is given in table B.11.

Table B.11: Golay (20,8) generator matrix

1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	1	0
0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	0	0	1
0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	0	1
0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	1
0	0	0	0	1	0	0	0	1	1	0	1	1	1	0	0	0	1	1	0
0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	1	1	1
0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	1	1	1	0
0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1	0	1	1

B.3.2 Quadratic residue (16,7,6)

The (16,7,6) is a shortened quadratic residue code is formed from the primitive (17,9,5) by deleting the first two information bits and extending by adding a single parity check bit to the end. The generator polynomial of the primitive (17,9,5) quadratic residue code is as follows:

$$G(x) = x^8 + x^5 + x^4 + x^3 + 1 = 471_8 \quad \text{(B.2)}$$

The generator matrix is given in table B.12.

Table B.12: Quadratic Residue (16,7,6) generator matrix

1	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1
0	1	0	0	0	0	0	1	0	0	0	1	1	1	1	0
0	0	1	0	0	0	0	1	1	0	1	1	0	1	1	1
0	0	0	1	0	0	0	1	1	1	1	0	0	0	1	0
0	0	0	0	1	0	0	1	1	1	0	0	1	0	0	1
0	0	0	0	0	1	0	0	1	1	1	0	0	1	0	1
0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	1

B.3.3 Hamming (17,12,3)

The (17,12,3) Hamming code is derived from shortening the primitive code generated from the polynomial g(x) given below:

$$g(x) = x^5 + x^2 + 1 = 45_8 \quad \text{(B.3)}$$

The generator matrix is given in table B.13.

Table B.13: Hamming (17,12,3) generator matrix

1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1
0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

B.3.4 Hamming (13,9,3), Hamming (15,11,3), and Hamming (16,11,4)

The generator matrices for the (16,11,4) Hamming code and the (13,9,3) Hamming code are derived from the (15,11,3) primitive Hamming code. The generator polynomial for the primitive code is as follows:

$$G(x) = x^4 + x + 1 = 23_8 \quad \text{(B.4)}$$

The generator matrices are given in tables B.14 to B.16.

Table B.14: Hamming (13,9,3) generator matrix

1	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0	0	0	0	0	0	0	1	1	1	0
0	0	1	0	0	0	0	0	0	0	1	1	1
0	0	0	1	0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	0	0	1	0	1	1
0	0	0	0	0	0	1	0	0	1	1	0	0
0	0	0	0	0	0	0	1	0	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	1	1

Table B.15: Hamming (15,11,3) generator matrix

1	0	0	0	0	0	0	0	0	0	0	1	0	0	1
0	1	0	0	0	0	0	0	0	0	0	1	1	0	1
0	0	1	0	0	0	0	0	0	0	0	1	1	1	1
0	0	0	1	0	0	0	0	0	0	0	1	1	1	0
0	0	0	0	1	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	0	0	0	1	0	1	1
0	0	0	0	0	0	0	0	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	1	0	0	1	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

Table B.16: Hamming (16,11,4) generator matrix

1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
0	1	0	0	0	0	0	0	0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1
0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0
0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1
0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1

B.3.5 Hamming (7,4,3)

The H(7,4,3) is a primitive Hamming code. The generator polynomial for the primitive code is as follows:

$$G(x) = x^3 + x + 1 = 13_8 \quad \text{(B.5)}$$

The generator matrix is given in table B.17.

Table B.17: Hamming (7,4,3) generator matrix

1	0	0	0	1	0	1
0	1	0	0	1	1	1
0	0	1	0	1	1	0
0	0	0	1	0	1	1

B.3.6 Reed-Solomon (12,9)

The Reed-Solomon code for the Link Control checksum is constructed over the GF(2^8) field. The (12,9,4) code is shortened from the (255,252,4) code by setting the first 243 message symbols for the code word to nulls (0). The generator polynomial of the (12,9,4) Reed-Solomon code is given by the following formula:

$$G(x) = (x + \alpha)\,(x + \alpha^2)\,(x + \alpha^3) \quad \text{(B.6)}$$

$$g(x) = x^3 + 0e\,x^2 + 38\,x + 40 \quad \text{(B.7)}$$

NOTE 1: Coefficients are in hexadecimal radix while exponents are in decimal radix.

The generator matrix is easily constructed from the generator polynomial. In the case of the Reed-Solomon code, the generator matrix uses GF(2^8) symbols of 8 bits each.

Table B.18: Reed-Solomon (12,9) generator matrix

01	00	00	00	00	00	00	00	00	1C	BC	FD
00	01	00	00	00	00	00	00	00	89	31	08
00	00	01	00	00	00	00	00	00	AD	41	36
00	00	00	01	00	00	00	00	00	7D	71	16
00	00	00	00	01	00	00	00	00	F3	A6	3A
00	00	00	00	00	01	00	00	00	08	83	7B
00	00	00	00	00	00	01	00	00	3F	6F	02
00	00	00	00	00	00	00	01	00	6C	0D	A7
00	00	00	00	00	00	00	00	01	0E	38	40

Calculation of the three parity bytes using the generator matrix method is summarized in the following formulas:

$$c = m \times G \quad \text{(B.8)}$$

where the arithmetic is done in GF(2^8), with:

$$m = (m_{K-1}, m_{K-2}, ... m_0) \quad (B.9)$$

$$c = (m_{K-1}, m_{K-2}, ... m_0, p_2, p_1, p_0) \quad (B.10)$$

where:

- m = message vector of K octets where K = 9;
- G = generator matrix, K rows by N columns;
- c = code word vector of N octets where N = 12.

The elements in GF(2^8) can be expressed in two ways, either as a polynomial in α with degree 7 or less, or as an exponent of α where the exponent is in the range 0 to 254 decimal.

NOTE 2: The zero element of the field does not have an exponential representation, so exponents only range up to 254 decimal.

Arithmetic in GF(2^8) consists of addition and multiplication. Addition is easy for the polynomial form since each term adds, modulo 2. Addition is hard for the exponent form since the exponent form is converted to a polynomial for addition and converted back to an exponent. Multiplication is easy for the exponent form since the exponents add modulo 255. Multiplication is harder for the polynomial form, since the polynomials have to be multiplied to yield a higher degree polynomial, and this has to be reduced to a residue modulo:

$$\alpha^8 + \alpha^4 + \alpha^3 + \alpha^2 + 1 \quad (B.11)$$

with

$$\alpha^e = b_7 \alpha^7 + b_6 \alpha^6 + ... b_1 \alpha + b_0 \quad (B.12)$$

where:

- e = exponent expressed in decimal radix;
- b = hexadecimal representation of bits (b_7, b_6, ... b_1, b_0).

These operations can be performed using the exponential and logarithm lookup tables B.19 and B.20. In these tables the exponents are given as decimal numbers and the polynomials are expressed as hexadecimal numbers.

Table B.19 is a table of polynomials that can be used to transform exponentials to polynomials.

Table B.19: Exponential table: B = α^E

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	2	4	8	10	20	40	80	1D	3A	74	E8	CD	87	13	26
16	4C	98	2D	5A	B4	75	EA	C9	8F	03	06	0C	18	30	60	C0
32	9D	27	4E	9C	25	4A	94	35	6A	D4	B5	77	EE	C1	9F	23
48	46	8C	05	0A	14	28	50	A0	5D	BA	69	D2	B9	6F	DE	A1
64	5F	BE	61	C2	99	2F	5E	BC	65	CA	89	0F	1E	3C	78	F0
80	FD	E7	D3	BB	6B	D6	B1	7F	FE	E1	DF	A3	5B	B6	71	E2
96	D9	AF	43	86	11	22	44	88	0D	1A	34	68	D0	BD	67	CE
112	81	1F	3E	7C	F8	ED	C7	93	3B	76	EC	C5	97	33	66	CC
128	85	17	2E	5C	B8	6D	DA	A9	4F	9E	21	42	84	15	2A	54
144	A8	4D	9A	29	52	A4	55	AA	49	92	39	72	E4	D5	B7	73
160	E6	D1	BF	63	C6	91	3F	7E	FC	E5	D7	B3	7B	F6	F1	FF
176	E3	DB	AB	4B	96	31	62	C4	95	37	6E	DC	A5	57	AE	41
192	82	19	32	64	C8	8D	07	0E	1C	38	70	E0	DD	A7	53	A6
208	51	A2	59	B2	79	F2	F9	EF	C3	9B	2B	56	AC	45	8A	09
224	12	24	48	90	3D	7A	F4	F5	F7	F3	FB	EB	CB	8B	0B	16
240	2C	58	B0	7D	FA	E9	CF	83	1B	36	6C	D8	AD	47	8E	01

Table B.20 is a table of exponentials that can be used to transform polynomials to exponentials.

Table B.20: Log table: E = LOG(B)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	--	0	1	25	2	50	26	198	3	223	51	238	27	104	199	75
10	4	100	224	14	52	141	239	129	28	193	105	248	200	8	76	113
20	5	138	101	47	225	36	15	33	53	147	142	218	240	18	130	69
30	29	181	194	125	106	39	249	185	201	154	9	120	77	228	114	166
40	6	191	139	98	102	221	48	253	226	152	37	179	16	145	34	136
50	54	208	148	206	143	150	219	189	241	210	19	92	131	56	70	64
60	30	66	182	163	195	72	126	110	107	58	40	84	250	133	186	61
70	202	94	155	159	10	21	121	43	78	212	229	172	115	243	167	87
80	7	112	192	247	140	128	99	13	103	74	222	237	49	197	254	24
90	227	165	153	119	38	184	180	124	17	68	146	217	35	32	137	46
A0	55	63	209	91	149	188	207	205	144	135	151	178	220	252	190	97
B0	242	86	211	171	20	42	93	158	132	60	57	83	71	109	65	162
C0	31	45	67	216	183	123	164	118	196	23	73	236	127	12	111	246
D0	108	161	59	82	41	157	85	170	251	96	134	177	187	204	62	90
E0	203	89	95	176	156	169	160	81	11	245	22	235	122	117	44	215
F0	79	174	213	233	230	231	173	232	116	214	244	234	168	80	88	175

B.3.7 8-bit CRC calculation

The 8-bit parity field for both the 4-burst CACH Short LC message and the Hash Address information element of the Activity Update Short LC message shall be an 8-bit CRC. It shall be the remainder of the division (modulo 2) by the generator polynomial:

$$G_8(x) = x^8 + x^2 + x + 1 \quad \text{(B.13)}$$

of the product of x^8 multiplied by the content of the data polynomial M(x). For the 8-bit CRC calculation there is no inversion polynomial and the initial remainder shall be 00000000_2.

For the Short LC, consider the 28 bits (SLCO and Data information elements as defined in clause 7.1 of the present document) as the message polynomial, M(x), of degree 27, with:

- bit 3 of octet 0 corresponding to the x^{27} term;
- bit 2 of octet 0 corresponding to the x^{26} term, etc.;
- bit 1 of octet 3 corresponding to the x^1 term;
- bit 0 of octet 3 corresponding to the x^0 term.

For the Hash ID information element consider the 24 bits of the destination address as the message polynomial, M(x), of degree 23, with:

- MSB of destination address corresponding to the x^{23} term, etc.;
- LSB of destination address corresponding to the x^0 term.

NOTE: Hash ID information element is defined in ETSI TS 102 361-2 [5].

The 8-bit CRC polynomial, $F_8(x)$, shall be computed from the formula:

$$F_8(x) = x^8\, M(x) \bmod G_8(x) \quad \text{(B.14)}$$

modulo 2, i.e. in GF(2).

For the Short LC the coefficients of $F_8(x)$ are placed in the CRC field with the MSB of the CRC corresponding to x^7 and the LSB of the CRC corresponding x^0. For the Hash ID information element the MSB of the CRC corresponds to the MSB of the Hash ID and the LSB of the CRC corresponds to the LSB of the Hash ID.

B.3.8 CRC-CCITT calculation

Consider the n data bits as the coefficients of a polynomial M(x) of degree n-1, associating the MSB of the zero-th octet with x^{n-1} and the LSB of the last octet with x^0. Define the generator polynomial, $G_H(x)$, and the inversion polynomial, $I_H(x)$.

$$G_H(x) = x^{16} + x^{12} + x^5 + 1 \quad \text{(B.15)}$$

$$I_H(x) = x^{15} + x^{14} + x^{13} + ... + x^2 + x + 1 \quad \text{(B.16)}$$

The CRC polynomial, $F_H(x)$, is then computed from the formula:

$$F_H(x) = (x^{16} M(x) \bmod G_H(x)) + I_H(x) \quad \text{(B.17)}$$

modulo 2, i.e. in GF(2).

The coefficients of $F_H(x)$ are placed in the CRC field with the MSB of the zero-th octet of the CRC corresponding to x^{15} and the LSB of the next octet of the CRC corresponding to x^0. For the CRC-CCITT calculation the initial remainder shall be 0000_{16}.

B.3.9 32-bit CRC calculation

The message CRC is a 4-octet cyclic redundancy check coded over all of the user data and pad octets included in the Intermediate Blocks and the Last Block. The message CRC does not include the Data Block Serial Number or the Block 9-bit CRC. The specific calculation is as follows:

The user data and pad bits begin as an arrangement of 16-bit words as illustrated in figure B.8AA. Each 16-bit word comprises a Most Significant Octet (MSO) and a Least Significant Octet (LSO).

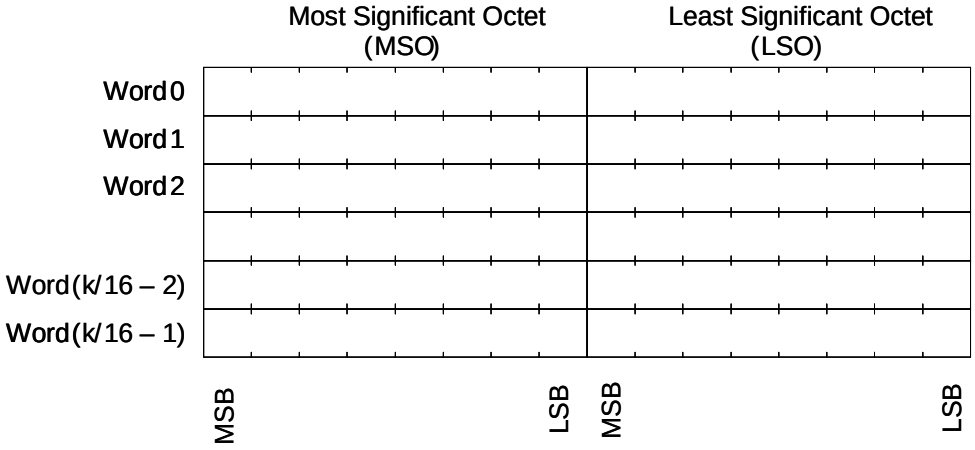


Figure B.8AA: User data and pad octets arranged as 16-bit words

The first octet of user data (8-bit character) shall be loaded into the MSO of Word 0, then the second octet of user data shall be loaded into the LSO of Word 0. The third octet of user data shall be loaded into the MSO of Word 1 and this continues until the LSO of Word k/16 - 1 is loaded last.

Let k be the total number of user data and pad bits over which the message CRC is to be calculated. To compute the 32-bit CRC, the 16-bit words are arranged linearly using the following format, where the least significant octet of a word appears before the most significant octet of the same word. This is illustrated in figure B.8B.

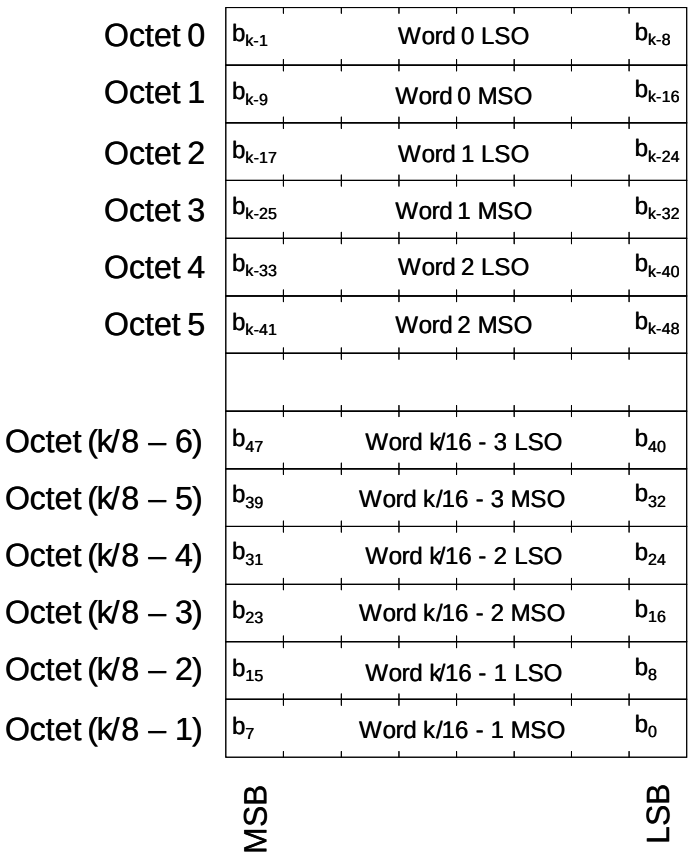


Figure B.8B: User data and pad octets arranged as 8-bit words in linear format

Now, consider the k message bits as the coefficients of a polynomial M(x) of degree k-1, associating the MSB of the zero-th octet with x^{k-1} and the LSB of the last octet with x^0. Define the generator polynomial, $G_M(x)$

$$G_M(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \qquad (B.18)$$

The message CRC polynomial, $F_M(x)$, is then computed from the following formula:

$$F_M(x) = x^{32}\, M(x) \bmod G_M(x) \qquad (B.19)$$

modulo 2, i.e. in GF(2). For the 32-bit CRC calculation the initial remainder shall be 00000000_{16}.

The coefficients of $F_M(x)$ are placed in the CRC field with the MSB of the 3rd octet of the CRC (i.e. the least significant CRC octet) corresponding to x^{31}, the MSB of the 2nd octet of the CRC corresponding to x^{23} , the MSB of the 1st octet of the CRC corresponding to x^{15}, and the MSB of the 0th octet of the CRC (i.e. the most significant CRC octet) corresponding to x^7. This ordering of CRC octets, where less significant octets appear before more significant octets, is shown in figure B.8C.

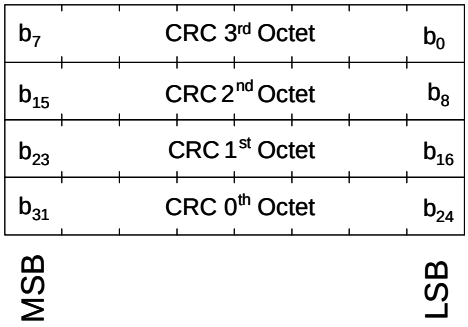


Figure B.8C: Ordering of CRC octets

B.3.10 CRC-9 calculation

For confirmed data blocks the transmitter computes the CRC-9 as follows. First, the block data and the seven bits of the serial number are arranged as a sequence of bits, with the serial number being the last seven bits. For a non-last data block the block data is the user data. For a last data block the block data is the user data and the message CRC. The CRC-9 calculation applies to the following block data sizes.

- Rate ½ coded confirmed (10 data octets): 80 bit sequence.
- Rate ¾ coded confirmed (16 data octets): 128 bit sequence.
- Rate 1 coded confirmed (22 data octets): 176 bit sequence.

The naming convention of the block data bits for a Rate ¾ coded confirmed data block is illustrated in figure B.8D.

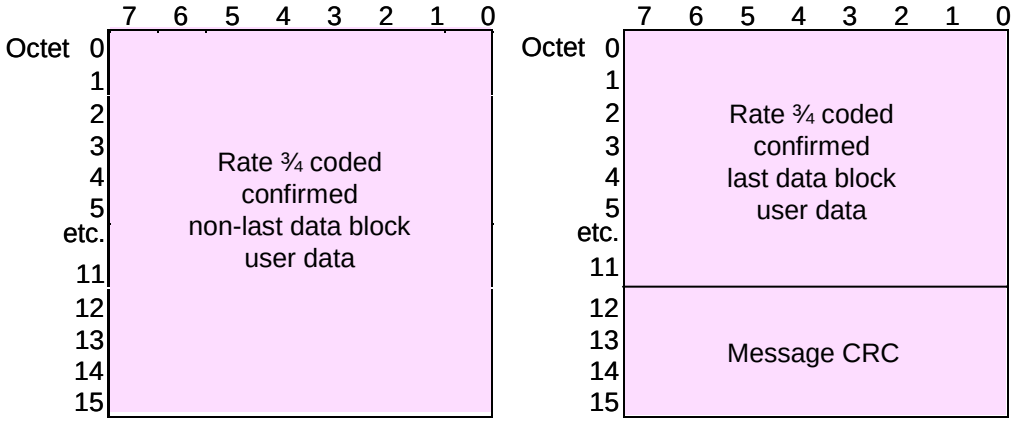


Figure B.8D: Rate ¾ coded confirmed user data bit numbering

The sequence of bits is then considered to be the coefficients of a message polynomial, M(x). M(x) will be of degree 134 for rate ¾ coded confirmed data blocks and M(x) will be of degree 86 for rate ½ coded confirmed data blocks and M(x) will be of degree 182 for rate 1 coded confirmed data blocks. For example M(x) for the rate ¾ coded confirmed data block case is:

- bit 7 of block data octet 0 corresponding to a coefficient of the x^{134} term;
- bit 6 of block data octet 0 corresponding to the x^{133} term;
- etc.
- bit 1 of block data octet 15 corresponding to the x^8 term;
- bit 0 of block data octet 15 corresponding to the x^7 term;
- bit 6 of the Serial Number corresponding to the x^6 term;
- bit 5 of the Serial Number corresponding to the x^5 term;
- etc.
- bit 1 of the Serial Number corresponding to the x^1 term;
- bit 0 of the Serial Number corresponding to the x^0 term.

Define the generator polynomial, $G_9(x)$, and the inversion polynomial, $I_9(x)$:

$$G_9(x) = x^9 + x^6 + x^4 + x^3 + 1 \quad \text{(B.20)}$$

$$I_9(x) = x^8 + x^7 + x^6 + ...+ x + 1 \quad \text{(B.21)}$$

The CRC-9 polynomial, $F_9(x)$, shall be computed from the formula:

$$F_9(x) = (x^9 M(x) \bmod G_9(x)) + I_9(x) \quad \text{(B.22)}$$

modulo 2, i.e. in GF(2).

The coefficients of $F_9(x)$ are placed in the CRC-9 field as illustrated in figure 8.12 of the present document with the MSB corresponding to bit 0 of octet 0, the next most significant bit corresponding to bit 7 of octet 1, and the LSB corresponding to bit 0 of octet 1. For the CRC-9 calculation the initial remainder shall be 000000000_2.

B.3.11 5-bit Checksum (CS) calculation

The calculation for the 5-bit CS is given by formula (B.23), where the summation is done with unsigned arithmetic in a 16-bit accumulator (maximum value is 9 × 255 = 2 295) where the values for LC_x are the octets of the 72-bit LC as shown in figure B.3. The calculation yields a 5-bit CS in the range 0 to 30.

$$CS = [LC\_0 + LC\_1 + ... + LC\_8] \bmod 31 \quad \text{(B.23)}$$

B.3.12 Data Type CRC Mask

A unique Data Type CRC Mask shall be applied to the entire CRC portion of the data or control burst information contents and is defined in table B.21. For transmission, the CRC mask shall be applied after the CRC calculation and before the FEC encoding. Application shall involve the exclusive-or operation of the calculated CRC and the CRC mask and then replacement of the calculated CRC with the exclusive-or result. For reception, the CRC mask shall be applied after the FEC decoding and before the CRC check. Application shall involve the exclusive-or operation of the received CRC and the CRC mask and replacement of the received CRC with the exclusive-or result. Use of the same mask at both transmission and reception results in the original calculated CRC at the receiver. Use of different masks results in a receiver CRC failure.

Table B.21: Data Type CRC Mask

Data Type	CRC mask
PI Header	6969_{16}
Voice LC Header	969696_{16}
Terminator with LC	999999_{16}
CSBK	$A5A5_{16}$
MBC Header	$AAAA_{16}$
MBC Continuation, see note 1	-
Data Header	$CCCC_{16}$
Rate ½ Data, see note 2	$0FO_{16}$
Rate ¾ Data, see note 2	$1FF_{16}$
Rate 1 Data, see note 2	$10F_{16}$
Idle, see note 1	-
Reverse Channel, see note 3	
NOTE 1: Not required. NOTE 2: Only used when CRC-9 present in burst. NOTE 3: Selected to minimize falsing between RC and sync patterns.	

The CRC mask values in table B.21 were selected for the appropriate CRC length from the values found in table B.22. Future values are to be selected from table B.22 so the minimum distance between CRC masks is preserved.

NOTE: The 9 bit CRC Mask values shown in table B.22 are shown in hexadecimal form. The 9 bit CRC Mask is composed of the 9 LSBs of the 12 bit value.

Table B.22: CRC Mask

Index	8 bit CRC	9 bit CRC	16 bit CRC	24 bit CRC	32 bit CRC
0	69_{16}	169_{16}	6969_{16}	696969_{16}	69696969_{16}
1	96_{16}	096_{16}	9696_{16}	969696_{16}	96969696_{16}
2	99_{16}	199_{16}	9999_{16}	999999_{16}	99999999_{16}
3	$A5_{16}$	$1A5_{16}$	$A5A5_{16}$	$A5A5A5_{16}$	$A5A5A5A5_{16}$
4	AA_{16}	$0AA_{16}$	$AAAA_{16}$	$AAAAAA_{16}$	$AAAAAAAA_{16}$
5	$C3_{16}$	$1C3_{16}$	$C3C3_{16}$	$C3C3C3_{16}$	$C3C3C3C3_{16}$
6	CC_{16}	$0CC_{16}$	$CCCC_{16}$	$CCCCCC_{16}$	$CCCCCCCC_{16}$
7	$F0_{16}$	$0F0_{16}$	$F0F0_{16}$	$F0F0F0_{16}$	$F0F0F0F0_{16}$
8	FF_{16}	$1FF_{16}$	$FFFF_{16}$	$FFFFFF_{16}$	$FFFFFFFF_{16}$
9	00_{16}	000_{16}	0000_{16}	000000_{16}	00000000_{16}
10	$0F_{16}$	$10F_{16}$	$0F0F_{16}$	$0F0F0F_{16}$	$0F0F0F0F_{16}$
11	33_{16}	133_{16}	3333_{16}	333333_{16}	33333333_{16}
12	$3C_{16}$	$03C_{16}$	$3C3C_{16}$	$3C3C3C_{16}$	$3C3C3C3C_{16}$
13	55_{16}	155_{16}	5555_{16}	555555_{16}	55555555_{16}
14	$5A_{16}$	$05A_{16}$	$5A5A_{16}$	$5A5A5A_{16}$	$5A5A5A5A_{16}$
15	66_{16}	066_{16}	6666_{16}	666666_{16}	66666666_{16}

B.3.13 7-bit CRC calculation

The 7-bit parity field for the RC Info shall be a 7-bit CRC. It shall be the remainder of the division (modulo 2) by the generator polynomial:

$$G_7(x) = x^7 + x^5 + x^2 + x + 1 \quad \text{(B.24)}$$

of the product of x^7 multiplied by the content of the data polynomial M(x). For the 7-bit CRC calculation there is no inversion polynomial and the initial remainder shall be 0000000_2.

For the Reverse channel, consider the 4 bits (RC info payload information elements as defined in table 9.6 of the present document) as the message polynomial, M(x), of degree 3, with:

- bit 3 of RC info corresponding to the x^3 term;
- bit 2 of RC info corresponding to the x^2 term;
- bit 1 of RC info corresponding to the x^1 term;
- bit 0 of RC info corresponding to the x^0 term.

NOTE: RC info information element is defined in ETSI TS 102 361-4 [11].

The 7-bit CRC polynomial, $F_7(x)$, shall be computed from the formula:

$$F_7(x) = x^7\ M(x) \bmod G_7(x) \quad \text{(B.25)}$$

modulo 2, i.e. in GF(2).

For the RC Info the coefficients of $F_7(x)$ are placed in the CRC field with the MSB of the CRC corresponding to x^6 and the LSB of the CRC corresponding x^0.

B.4 Interleaving

B.4.1 CACH interleaving

The details for interleaving the payload and CACH framing over a 24-bit CACH burst are shown in figure B.9. The access (AT), numbering (TC), and framing bits (LCSS) and their three Hamming parity bits (H) are spread over the entire CACH burst for resistance to fades. The seventeen CACH payload bits (P) placed sequentially in the gaps.

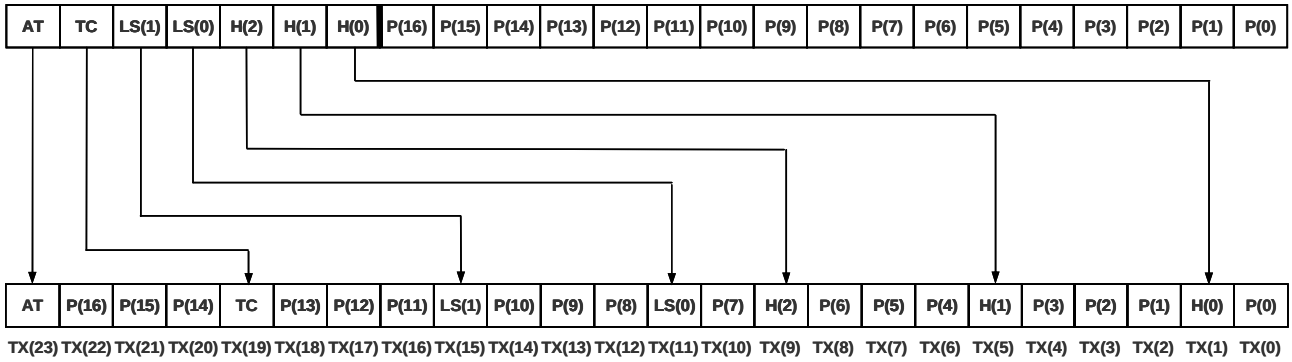


Figure B.9: CACH burst interleaver

Annex C (informative): Example timing diagrams

C.0 General

This annex describes and shows some timing examples.

C.1 Direct mode timing

In this case a mobile station transmits a Normal Burst in Slot 1 and then listens for a RC burst in Slot 2. Alternatively, the mobile station transmits a Normal Burst in Slot 2 and listens for a RC Burst in Slot 1; the timing is the same either way. The timing is shown in figure C.1.

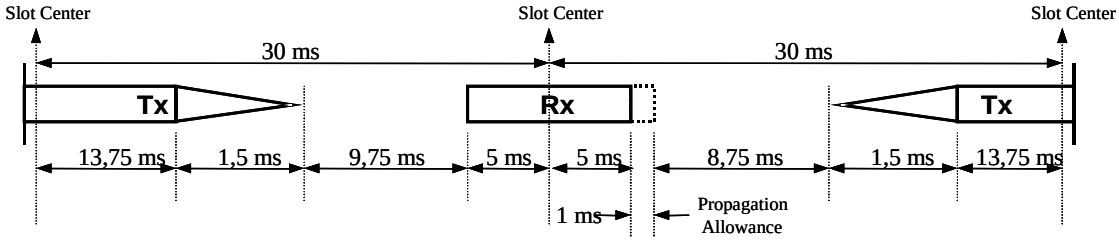


Figure C.1: Direct mode timing diagram

The case shown in figure C.1 is that of a mobile station transmitting in direct mode and then listening for a RC transmission from a second mobile station. Since the second mobile station can be a substantial distance from the first mobile station, its RC burst can be delayed with respect to the slotting structure defined by the first mobile station. By specification, the delay can be up to 1 ms. This means that the first mobile station is ready to receive the RC 9,75 ms after sending its Normal Burst but may change frequency to transmit no sooner than 8,75 ms before its next Normal Burst is to be sent. Therefore, in this case, the maximum synthesizer lock-time should be 8,75 ms.

C.2 Reverse Channel timing

This example shows a mobile station transmitting on a RC burst between receiving Normal Bursts from a second base or mobile station. In this case, the mobile station synchronizes its timing to the second station, regardless of whether the second station is a base or mobile, and, therefore, there is no timing offset due to propagation delay. The timing is shown in figure C.2. The maximum allowable synthesizer lock-time should be 8,75 ms.

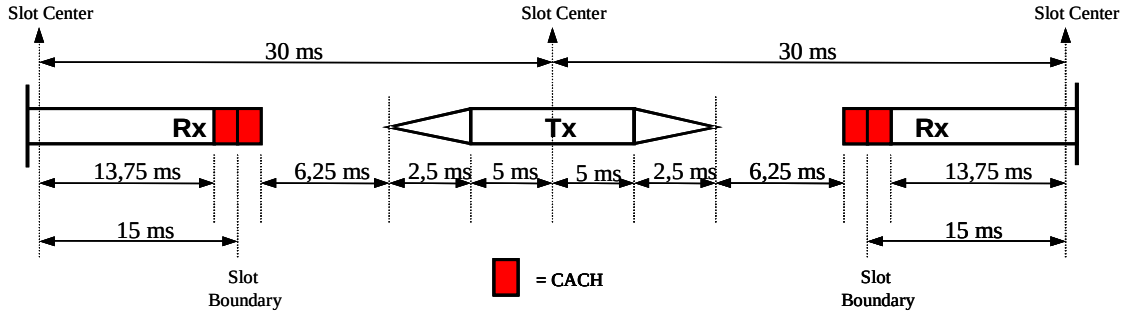


Figure C.2: Reverse Channel timing diagram

Annex D (normative): Idle and Null message bit definition

D.0 Idle and Null message bit definition - Introduction

The following abbreviations are used in the tables:

H_Cx	Hamming parity bit from column x of a BPTC;
H_Rx	Hamming parity bit from row x of a BPTC;
I	Information bit;
R	Reserved bit;
TX	Transmitted bit.

D.1 Null embedded message bit definitions

The 11 information bits of the Null embedded message are all set to 0. Consequently, all of the FEC and parity check bits of the BPTC will also be 0. The 32 bits of the Transmit Matrix defined in clause B.2.1 are listed in table D.1.

Table D.1: Null embedded signalling

Bit index	Bit value	Bit index	Bit value	Bit index	Bit value	Bit index	Bit value
TX(31)	0	TX(23)	0	TX(15)	0	TX(7)	0
TX(30)	0	TX(22)	0	TX(14)	0	TX(6)	0
TX(29)	0	TX(21)	0	TX(13)	0	TX(5)	0
TX(28)	0	TX(20)	0	TX(12)	0	TX(4)	0
TX(27)	0	TX(19)	0	TX(11)	0	TX(3)	0
TX(26)	0	TX(18)	0	TX(10)	0	TX(2)	0
TX(25)	0	TX(17)	0	TX(9)	0	TX(1)	0
TX(24)	0	TX(16)	0	TX(8)	0	TX(0)	0

D.2 Idle message bit definitions

The information bits for the Idle message are creating by generating 96 bits of pseudo random bits. The specific values of these bits are given in table D.2.

Table D.2: Information bits for Idle message

Bit name	Bit value	Bit name	Bit value	Bit name	Bit value	Bit name	Bit value
I(95)	1	I(71)	0	I(47)	0	I(23)	1
I(94)	1	I(70)	0	I(46)	1	I(22)	1
I(93)	1	I(69)	0	I(45)	0	I(21)	0
I(92)	1	I(68)	1	I(44)	0	I(20)	0
I(91)	1	I(67)	0	I(43)	1	I(19)	1
I(90)	1	I(66)	1	I(42)	1	I(18)	1
I(89)	1	I(65)	1	I(41)	1	I(17)	0
I(88)	1	I(64)	1	I(40)	0	I(16)	1
I(87)	1	I(63)	0	I(39)	1	I(15)	1
I(86)	0	I(62)	0	I(38)	1	I(14)	0
I(85)	0	I(61)	1	I(37)	0	I(13)	0
I(84)	0	I(60)	1	I(36)	1	I(12)	0
I(83)	0	I(59)	0	I(35)	0	I(11)	1
I(82)	0	I(58)	0	I(34)	0	I(10)	0
I(81)	1	I(57)	1	I(33)	0	I(9)	1
I(80)	1	I(56)	0	I(32)	1	I(8)	0
I(79)	1	I(55)	0	I(31)	1	I(7)	1
I(78)	1	I(54)	0	I(30)	1	I(6)	0
I(77)	0	I(53)	0	I(29)	1	I(5)	0
I(76)	1	I(52)	0	I(28)	0	I(4)	1
I(75)	1	I(51)	1	I(27)	0	I(3)	0
I(74)	1	I(50)	0	I(26)	1	I(2)	0
I(73)	1	I(49)	0	I(25)	1	I(1)	0
I(72)	1	I(48)	1	I(24)	1	I(0)	1

The information bits are then FEC encoded using the BPTC (196,96) defined in clause B.1.1 and interleaved for the general data burst. The information bits and FEC parity check bits after encoding are shown in figure D.1 which follows the format defined in figure B.1.

0	0	0	1	1	1	1	1	1	1	1	0	1	0	0
1	0	0	0	0	0	1	1	1	1	0	1	1	0	1
1	1	1	1	1	0	0	0	1	0	1	1	1	0	1
1	1	0	0	1	1	0	0	1	0	0	0	1	0	1
0	0	0	1	0	0	1	0	1	0	0	0	1	1	1
1	1	1	0	1	1	0	1	0	0	0	1	1	0	1
1	1	1	1	0	0	1	1	1	1	1	0	0	1	0
0	0	1	1	0	1	1	0	0	0	1	1	1	0	1
0	1	0	1	0	0	1	0	0	0	1	0	1	0	1
0	1	0	0	1	1	1	0	0	1	0	0	0	1	1
1	0	1	1	0	0	1	1	1	1	0	1	1	0	0
0	0	1	0	0	0	0	1	0	0	0	0	1	0	0
0	1	0	0	1	0	1	0	1	1	1	0	1	1	0

Figure D.1: FEC encoded Idle message

The specific bit names and their corresponding bit values for the information and FEC parity bits are listed in table D.3.

Table D.3: FEC encoded bits for Idlemessage

Bit name	Bit value	Bit name	Bit value	Bit name	Bit value	Bit name	Bit value
R(3)	0	I(62)	0	I(25)	1	H_C12(3)	0
R(2)	0	I(61)	1	I(24)	1	H_C13(3)	0
R(1)	0	I(60)	1	I(23)	1	H_C14(3)	1
R(0)	0	I(59)	0	I(22)	1	H_C15(3)	1
I(95)	1	I(58)	0	H_R7(3)	0	H_C1(2)	1
I(94)	1	I(57)	1	H_R7(2)	0	H_C2(2)	0
I(93)	1	I(56)	0	H_R7(1)	1	H_C3(2)	1
I(92)	1	I(55)	0	H_R7(0)	0	H_C4(2)	1
I(91)	1	H_R4(3)	0	I(21)	0	H_C5(2)	0
I(90)	1	H_R4(2)	1	I(20)	0	H_C6(2)	0
I(89)	1	H_R4(1)	0	I(19)	1	H_C7(2)	1
I(88)	1	H_R4(0)	1	I(18)	1	H_C8(2)	1
H_R1(3)	0	I(54)	0	I(17)	0	H_C9(2)	1
H_R1(2)	1	I(53)	0	I(16)	1	H_C10(2)	1
H_R1(1)	0	I(52)	0	I(15)	1	H_C11(2)	0
H_R1(0)	0	I(51)	1	I(14)	0	H_C12(2)	1
I(87)	1	I(50)	0	I(13)	0	H_C13(2)	1
I(86)	0	I(49)	0	I(12)	0	H_C14(2)	0
I(85)	0	I(48)	1	I(11)	1	H_C15(2)	0
I(84)	0	I(47)	0	H_R8(3)	1	H_C1(1)	0
I(83)	0	I(46)	1	H_R8(2)	1	H_C2(1)	0
I(82)	0	I(45)	0	H_R8(1)	0	H_C3(1)	1
I(81)	1	I(44)	0	H_R8(0)	1	H_C4(1)	0
I(80)	1	H_R5(3)	0	I(10)	0	H_C5(1)	0
I(79)	1	H_R5(2)	1	I(9)	1	H_C6(1)	0
I(78)	1	H_R5(1)	1	I(8)	0	H_C7(1)	0
I(77)	0	H_R5(0)	1	I(7)	1	H_C8(1)	1
H_R2(3)	1	I(43)	1	I(6)	0	H_C9(1)	0
H_R2(2)	1	I(42)	1	I(5)	0	H_C10(1)	0
H_R2(1)	0	I(41)	1	I(4)	1	H_C11(1)	0
H_R2(0)	1	I(40)	0	I(3)	0	H_C12(1)	0
I(76)	1	I(39)	1	I(2)	0	H_C13(1)	1
I(75)	1	I(38)	1	I(1)	0	H_C14(1)	0
I(74)	1	I(37)	0	I(0)	1	H_C15(1)	0
I(73)	1	I(36)	1	H_R9(3)	0	H_C1(0)	0
I(72)	1	I(35)	0	H_R9(2)	1	H_C2(0)	1
I(71)	0	I(34)	0	H_R9(1)	0	H_C3(0)	0
I(70)	0	I(33)	0	H_R9(0)	1	H_C4(0)	0
I(69)	0	H_R6(3)	1	H_C1(3)	0	H_C5(0)	1
I(68)	1	H_R6(2)	1	H_C2(3)	1	H_C6(0)	0
I(67)	0	H_R6(1)	0	H_C3(3)	0	H_C7(0)	1
I(66)	1	H_R6(0)	1	H_C4(3)	0	H_C8(0)	0
H_R3(3)	1	I(32)	1	H_C5(3)	1	H_C9(0)	1
H_R3(2)	1	I(31)	1	H_C6(3)	1	H_C10(0)	1
H_R3(1)	0	I(30)	1	H_C7(3)	1	H_C11(0)	1
H_R3(0)	1	I(29)	1	H_C8(3)	0	H_C12(0)	0
I(65)	1	I(28)	0	H_C9(3)	0	H_C13(0)	1
I(64)	1	I(27)	0	H_C10(3)	1	H_C14(0)	1
I(63)	0	I(26)	1	H_C11(3)	0	H_C15(0)	0

Annex E (normative): Transmit bit order

Tables E.1 to E.12 list out the transmit order of bits for the basic data and voice bursts. The transmitter modulation consists of a sequence of dibit symbols that are serially transmitted. Each dibit consists of 2 bits of information. The tables for the bursts consist of a sequence of dibit symbols, starting with symbol L66 (66 symbols to the left of burst centre), decrementing to L1, then proceeding with R1, and then incrementing up to R66 (66 symbols to the right of burst centre). The first symbol transmitted shall be symbol L66.

The transmitted signal consists of a sequence of fields of information. Each field is in turn decomposed into bits. For example, the voice code word 0, or c_0, consists of 24 bits which are numbered 23, 22, 21, ... 1, 0. The least significant bit is always numbered 0 in a field. Generally, the least significant bit is always transmitted last. The least significant bit is always portrayed as the right-most bit. The number of the bit is always enclosed in parenthesis, for example HC_12(1) refers to the vector for the Hamming code word for the 12^{th} column, first bit.

After most of the information fields there is a parity check field for the error correcting code. The name of the code is always used to denote the parity check field. For example, a QR code is used to protect the embedded code word (EMB), so the parity check field is named qr(x) where x varies from 8 down to 0. Bit 0 is always the least significant bit of the parity check field, and is always portrayed as the right-most bit. In most cases, an index number for a bit follows the field name, as in "H_C11(3)", which denotes bit 3 of the field.

The following abbreviations are used in the tables:

CC	Colour Code;
D_Sync	General Data Burst Sync;
DT	Data Type field for General Data Bursts;
Golay	Golay Code parity check;
H_Cx	Hamming parity bit from column x of a BPTC;
H_Rx	Hamming parity bit from row x of a BPTC;
Hx	Hamming parity bit for row x of a BPTC;
I	Information bit for General Data Burst payload;
LCSS	Link Control Start/ Stop;
N_LC	Null LC bit;
PC	Parity Check bit;
PI	Pre-emption and power control Indicator;
QR	Quadratic Residue Code Parity Check bit;
R	Reserved bit;
R_Sync	Reverse Channel Sync;
RC	Reverse Channel information bit;
Trellis_Dibit	Output Dibit from Trellis C ode;
V_Sync	TDMA Voice Burst Sync;
VS	Vocoder Socket bit.

Table E.1: Transmit bit order for BPTC general data burst with SYNC

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	R(3)	H_R1(2)	L22	H_C14(2)	H_C12(1)	R23	I(75)	H_R3(0)
L65	I(77)	I(68)	L21	H_C10(0)	I(92)	R24	H_R4(2)	I(44)
L64	I(59)	I(50)	L20	I(83)	I(74)	R25	I(35)	I(26)
L63	I(41)	I(32)	L19	I(65)	H_R4(1)	R26	I(17)	I(8)
L62	H_R7(1)	H_R8(3)	L18	H_R5(3)	I(34)	R27	H_C1(3)	H_C14(3)
L61	I(1)	H_C8(3)	L17	CC(3)	CC(2)	R28	H_C12(2)	H_C10(1)
L60	H_C6(2)	H_C4(1)	L16	CC(1)	CC(0)	R29	H_C8(0)	I(94)
L59	H_C2(0)	H_C15(0)	L15	DT (3)	DT (2)	R30	I(85)	I(76)
L58	H_R1(3)	I(78)	L14	DT (1)	DT (0)	R31	H_R3(1)	H_R4(3)
L57	I(69)	I(60)	L13	Golay(11)	Golay(10)	R32	I(45)	I(36)
L56	I(51)	I(42)	L12	D_Sync(47)	D_Sync(46)	R33	I(27)	I(18)
L55	H_R6(0)	H_R7(2)	L11	D_Sync(45)	D_Sync(44)	R34	I(9)	H_R9(0)
L54	I(11)	I(2)	L10	D_Sync(43)	D_Sync(42)	R35	H_C13(3)	H_C11(2)
L53	H_C7(3)	H_C5(2)	L9	D_Sync(41)	D_Sync(40)	R36	H_C9(1)	H_C7(0)
L52	H_C3(1)	H_C1(0)	L8	D_Sync(39)	D_Sync(38)	R37	I(95)	I(86)
L51	H_C14(0)	I(88)	L7	D_Sync(37)	D_Sync(36)	R38	H_R2(0)	H_R3(2)
L50	I(79)	I(70)	L6	D_Sync(35)	D_Sync(34)	R39	I(55)	I(46)
L49	I(61)	I(52)	L5	D_Sync(33)	D_Sync(32)	R40	I(37)	I(28)
L48	I(43)	H_R6(1)	L4	D_Sync(31)	D_Sync(30)	R41	I(19)	I(10)
L47	H_R7(3)	I(12)	L3	D_Sync(29)	D_Sync(28)	R42	H_R9(1)	H_C12(3)
L46	I(3)	H_C6(3)	L2	D_Sync(27)	D_Sync(26)	R43	H_C10(2)	H_C8(1)
L45	H_C4(2)	H_C2(1)	L1	D_Sync(25)	D_Sync(24)	R44	H_C6(0)	R(0)
L44	H_C15(1)	H_C13(0)	R1	D_Sync(23)	D_Sync(22)	R45	I(87)	H_R2(1)
L43	I(89)	I(80)	R2	D_Sync(21)	D_Sync(20)	R46	H_R3(3)	I(56)
L42	I(71)	I(62)	R3	D_Sync(19)	D_Sync(18)	R47	I(47)	I(38)
L41	I(53)	H_R5(0)	R4	D_Sync(17)	D_Sync(16)	R48	I(29)	I(20)
L40	H_R6(2)	I(22)	R5	D_Sync(15)	D_Sync(14)	R49	H_R8(0)	H_R9(2)
L39	I(13)	I(4)	R6	D_Sync(13)	D_Sync(12)	R50	H_C11(3)	H_C9(2)
L38	H_C5(3)	H_C3(2)	R7	D_Sync(11)	D_Sync(10)	R51	H_C7(1)	H_C5(0)
L37	H_C1(1)	H_C14(1)	R8	D_Sync(9)	D_Sync(8)	R52	R(1)	H_R1(0)
L36	H_C12(0)	I(90)	R9	D_Sync(7)	D_Sync(6)	R53	H_R2(2)	I(66)
L35	I(81)	I(72)	R10	D_Sync(5)	D_Sync(4)	R54	I(57)	I(48)
L34	I(63)	I(54)	R11	D_Sync(3)	D_Sync(2)	R55	I(39)	I(30)
L33	H_R5(1)	H_R6(3)	R12	D_Sync(1)	D_Sync(0)	R56	I(21)	H_R8(1)
L32	I(23)	I(14)	R13	Golay(9)	Golay(8)	R57	H_R9(3)	H_C10(3)
L31	I(5)	H_C4(3)	R14	Golay(7)	Golay(6)	R58	H_C8(2)	H_C6(1)
L30	H_C2(2)	H_C15(2)	R15	Golay(5)	Golay(4)	R59	H_C4(0)	R(2)
L29	H_C13(1)	H_C11(0)	R16	Golay(3)	Golay(2)	R60	H_R1(1)	H_R2(3)
L28	I(91)	I(82)	R17	Golay(1)	Golay(0)	R61	I(67)	I(58)
L27	I(73)	I(64)	R18	I(25)	I(16)	R62	I(49)	I(40)
L26	H_R4(0)	H_R5(2)	R19	I(7)	H_C2(3)	R63	I(31)	H_R7(0)
L25	I(33)	I(24)	R20	H_C15(3)	H_C13(2)	R64	H_R8(2)	I(0)
L24	I(15)	I(6)	R21	H_C11(1)	H_C9(0)	R65	H_C9(3)	H_C7(2)
L23	H_C3(3)	H_C1(2)	R22	I(93)	I(84)	R66	H_C5(1)	H_C3(0)

Table E.2: Transmit bit order for BPTC general data burst with RC

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	R(3)	H_R1(2)	L22	H_C14(2)	H_C12(1)	R23	I(75)	H_R3(0)
L65	I(77)	I(68)	L21	H_C10(0)	I(92)	R24	H_R4(2)	I(44)
L64	I(59)	I(50)	L20	I(83)	I(74)	R25	I(35)	I(26)
L63	I(41)	I(32)	L19	I(65)	H_R4(1)	R26	I(17)	I(8)
L62	H_R7(1)	H_R8(3)	L18	H_R5(3)	I(34)	R27	H_C1(3)	H_C14(3)
L61	I(1)	H_C8(3)	L17	CC(3)	CC(2)	R28	H_C12(2)	H_C10(1)
L60	H_C6(2)	H_C4(1)	L16	CC(1)	CC(0)	R29	H_C8(0)	I(94)
L59	H_C2(0)	H_C15(0)	L15	DT (3)	DT (2)	R30	I(85)	I(76)
L58	H_R1(3)	I(78)	L14	DT (1)	DT (0)	R31	H_R3(1)	H_R4(3)
L57	I(69)	I(60)	L13	Golay(11)	Golay(10)	R32	I(45)	I(36)
L56	I(51)	I(42)	L12	CC(3)	CC(2)	R33	I(27)	I(18)
L55	H_R6(0)	H_R7(2)	L11	CC(1)	CC(0)	R34	I(9)	H_R9(0)
L54	I(11)	I(2)	L10	PI	LCSS(1)	R35	H_C13(3)	H_C11(2)
L53	H_C7(3)	H_C5(2)	L9	LCSS(0)	QR(8)	R36	H_C9(1)	H_C7(0)
L52	H_C3(1)	H_C1(0)	L8	RC(10)	PC(7)	R37	I(95)	I(86)
L51	H_C14(0)	I(88)	L7	RC(9)	PC(6)	R38	H_R2(0)	H_R3(2)
L50	I(79)	I(70)	L6	RC(8)	PC(5)	R39	I(55)	I(46)
L49	I(61)	I(52)	L5	RC(7)	PC(4)	R40	I(37)	I(28)
L48	I(43)	H_R6(1)	L4	RC(6)	PC(3)	R41	I(19)	I(10)
L47	H_R7(3)	I(12)	L3	RC(5)	PC(2)	R42	H_R9(1)	H_C12(3)
L46	I(3)	H_C6(3)	L2	RC(4)	PC(1)	R43	H_C10(2)	H_C8(1)
L45	H_C4(2)	H_C2(1)	L1	RC(3)	PC(0)	R44	H_C6(0)	R(0)
L44	H_C15(1)	H_C13(0)	R1	RC(2)	PC(15)	R45	I(87)	H_R2(1)
L43	I(89)	I(80)	R2	RC(1)	PC(14)	R46	H_R3(3)	I(56)
L42	I(71)	I(62)	R3	RC(0)	PC(13)	R47	I(47)	I(38)
L41	I(53)	H_R5(0)	R4	H1(4)	PC(12)	R48	I(29)	I(20)
L40	H_R6(2)	I(22)	R5	H1(3)	PC(11)	R49	H_R8(0)	H_R9(2)
L39	I(13)	I(4)	R6	H1(2)	PC(10)	R50	H_C11(3)	H_C9(2)
L38	H_C5(3)	H_C3(2)	R7	H1(1)	PC(9)	R51	H_C7(1)	H_C5(0)
L37	H_C1(1)	H_C14(1)	R8	H1(0)	PC(8)	R52	R(1)	H_R1(0)
L36	H_C12(0)	I(90)	R9	QR(7)	QR(6)	R53	H_R2(2)	I(66)
L35	I(81)	I(72)	R10	QR(5)	QR(4)	R54	I(57)	I(48)
L34	I(63)	I(54)	R11	QR(3)	QR(2)	R55	I(39)	I(30)
L33	H_R5(1)	H_R6(3)	R12	QR(1)	QR(0)	R56	I(21)	H_R8(1)
L32	I(23)	I(14)	R13	Golay(9)	Golay(8)	R57	H_R9(3)	H_C10(3)
L31	I(5)	H_C4(3)	R14	Golay(7)	Golay(6)	R58	H_C8(2)	H_C6(1)
L30	H_C2(2)	H_C15(2)	R15	Golay(5)	Golay(4)	R59	H_C4(0)	R(2)
L29	H_C13(1)	H_C11(0)	R16	Golay(3)	Golay(2)	R60	H_R1(1)	H_R2(3)
L28	I(91)	I(82)	R17	Golay(1)	Golay(0)	R61	I(67)	I(58)
L27	I(73)	I(64)	R18	I(25)	I(16)	R62	I(49)	I(40)
L26	H_R4(0)	H_R5(2)	R19	I(7)	H_C2(3)	R63	I(31)	H_R7(0)
L25	I(33)	I(24)	R20	H_C15(3)	H_C13(2)	R64	H_R8(2)	I(0)
L24	I(15)	I(6)	R21	H_C11(1)	H_C9(0)	R65	H_C9(3)	H_C7(2)
L23	H_C3(3)	H_C1(2)	R22	I(93)	I(84)	R66	H_C5(1)	H_C3(0)

Table E.3: Transmit bit order for rate ¾ data burst with SYNC

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	Trellis_Dibit(97)		L22	Trellis_Dibit(53)		R23	Trellis_Dibit(43)	
L65	Trellis_Dibit(96)		L21	Trellis_Dibit(52)		R24	Trellis_Dibit(42)	
L64	Trellis_Dibit(95)		L20	Trellis_Dibit(51)		R25	Trellis_Dibit(41)	
L63	Trellis_Dibit(94)		L19	Trellis_Dibit(50)		R26	Trellis_Dibit(40)	
L62	Trellis_Dibit(93)		L18	Trellis_Dibit(49)		R27	Trellis_Dibit(39)	
L61	Trellis_Dibit(92)		L17	CC(3)	CC(2)	R28	Trellis_Dibit(38)	
L60	Trellis_Dibit(91)		L16	CC(1)	CC(0)	R29	Trellis_Dibit(37)	
L59	Trellis_Dibit(90)		L15	DT (3)	DT (2)	R30	Trellis_Dibit(36)	
L58	Trellis_Dibit(89)		L14	DT (1)	DT (0)	R31	Trellis_Dibit(35)	
L57	Trellis_Dibit(88)		L13	Golay(11)	Golay(10)	R32	Trellis_Dibit(34)	
L56	Trellis_Dibit(87)		L12	D_Sync(47)	D_Sync(46)	R33	Trellis_Dibit(33)	
L55	Trellis_Dibit(86)		L11	D_Sync(45)	D_Sync(44)	R34	Trellis_Dibit(32)	
L54	Trellis_Dibit(85)		L10	D_Sync(43)	D_Sync(42)	R35	Trellis_Dibit(31)	
L53	Trellis_Dibit(84)		L9	D_Sync(41)	D_Sync(40)	R36	Trellis_Dibit(30)	
L52	Trellis_Dibit(83)		L8	D_Sync(39)	D_Sync(38)	R37	Trellis_Dibit(29)	
L51	Trellis_Dibit(82)		L7	D_Sync(37)	D_Sync(36)	R38	Trellis_Dibit(28)	
L50	Trellis_Dibit(81)		L6	D_Sync(35)	D_Sync(34)	R39	Trellis_Dibit(27)	
L49	Trellis_Dibit(80)		L5	D_Sync(33)	D_Sync(32)	R40	Trellis_Dibit(26)	
L48	Trellis_Dibit(79)		L4	D_Sync(31)	D_Sync(30)	R41	Trellis_Dibit(25)	
L47	Trellis_Dibit(78)		L3	D_Sync(29)	D_Sync(28)	R42	Trellis_Dibit(24)	
L46	Trellis_Dibit(77)		L2	D_Sync(27)	D_Sync(26)	R43	Trellis_Dibit(23)	
L45	Trellis_Dibit(76)		L1	D_Sync(25)	D_Sync(24)	R44	Trellis_Dibit(22)	
L44	Trellis_Dibit(75)		R1	D_Sync(23)	D_Sync(22)	R45	Trellis_Dibit(21)	
L43	Trellis_Dibit(74)		R2	D_Sync(21)	D_Sync(20)	R46	Trellis_Dibit(20)	
L42	Trellis_Dibit(73)		R3	D_Sync(19)	D_Sync(18)	R47	Trellis_Dibit(19)	
L41	Trellis_Dibit(72)		R4	D_Sync(17)	D_Sync(16)	R48	Trellis_Dibit(18)	
L40	Trellis_Dibit(71)		R5	D_Sync(15)	D_Sync(14)	R49	Trellis_Dibit(17)	
L39	Trellis_Dibit(70)		R6	D_Sync(13)	D_Sync(12)	R50	Trellis_Dibit(16)	
L38	Trellis_Dibit(69)		R7	D_Sync(11)	D_Sync(10)	R51	Trellis_Dibit(15)	
L37	Trellis_Dibit(68)		R8	D_Sync(9)	D_Sync(8)	R52	Trellis_Dibit(14)	
L36	Trellis_Dibit(67)		R9	D_Sync(7)	D_Sync(6)	R53	Trellis_Dibit(13)	
L35	Trellis_Dibit(66)		R10	D_Sync(5)	D_Sync(4)	R54	Trellis_Dibit(12)	
L34	Trellis_Dibit(65)		R11	D_Sync(3)	D_Sync(2)	R55	Trellis_Dibit(11)	
L33	Trellis_Dibit(64)		R12	D_Sync(1)	D_Sync(0)	R56	Trellis_Dibit(10)	
L32	Trellis_Dibit(63)		R13	Golay(9)	Golay(8)	R57	Trellis_Dibit(9)	
L31	Trellis_Dibit(62)		R14	Golay(7)	Golay(6)	R58	Trellis_Dibit(8)	
L30	Trellis_Dibit(61)		R15	Golay(5)	Golay(4)	R59	Trellis_Dibit(7)	
L29	Trellis_Dibit(60)		R16	Golay(3)	Golay(2)	R60	Trellis_Dibit(6)	
L28	Trellis_Dibit(59)		R17	Golay(1)	Golay(0)	R61	Trellis_Dibit(5)	
L27	Trellis_Dibit(58)		R18	Trellis_Dibit(48)		R62	Trellis_Dibit(4)	
L26	Trellis_Dibit(57)		R19	Trellis_Dibit(47)		R63	Trellis_Dibit(3)	
L25	Trellis_Dibit(56)		R20	Trellis_Dibit(46)		R64	Trellis_Dibit(2)	
L24	Trellis_Dibit(55)		R21	Trellis_Dibit(45)		R65	Trellis_Dibit(1)	
L23	Trellis_Dibit(54)		R22	Trellis_Dibit(44)		R66	Trellis_Dibit(0)	

Table E.4: Transmit bit order for rate ¾ data burst with Reverse Channel

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	Trellis_Dibit(97)		L22	Trellis_Dibit(53)		R23	Trellis_Dibit(43)	
L65	Trellis_Dibit(96)		L21	Trellis_Dibit(52)		R24	Trellis_Dibit(42)	
L64	Trellis_Dibit(95)		L20	Trellis_Dibit(51)		R25	Trellis_Dibit(41)	
L63	Trellis_Dibit(94)		L19	Trellis_Dibit(50)		R26	Trellis_Dibit(40)	
L62	Trellis_Dibit(93)		L18	Trellis_Dibit(49)		R27	Trellis_Dibit(39)	
L61	Trellis_Dibit(92)		L17	CC(3)	CC(2)	R28	Trellis_Dibit(38)	
L60	Trellis_Dibit(91)		L16	CC(1)	CC(0)	R29	Trellis_Dibit(37)	
L59	Trellis_Dibit(90)		L15	DT (3)	DT (2)	R30	Trellis_Dibit(36)	
L58	Trellis_Dibit(89)		L14	DT (1)	DT (0)	R31	Trellis_Dibit(35)	
L57	Trellis_Dibit(88)		L13	Golay(11)	Golay(10)	R32	Trellis_Dibit(34)	
L56	Trellis_Dibit(87)		L12	CC(3)	CC(2)	R33	Trellis_Dibit(33)	
L55	Trellis_Dibit(86)		L11	CC(1)	CC(0)	R34	Trellis_Dibit(32)	
L54	Trellis_Dibit(85)		L10	PI	LCSS(1)	R35	Trellis_Dibit(31)	
L53	Trellis_Dibit(84)		L9	LCSS(0)	QR(8)	R36	Trellis_Dibit(30)	
L52	Trellis_Dibit(83)		L8	RC(10)	PC(7)	R37	Trellis_Dibit(29)	
L51	Trellis_Dibit(82)		L7	RC(9)	PC(6)	R38	Trellis_Dibit(28)	
L50	Trellis_Dibit(81)		L6	RC(8)	PC(5)	R39	Trellis_Dibit(27)	
L49	Trellis_Dibit(80)		L5	RC(7)	PC(4)	R40	Trellis_Dibit(26)	
L48	Trellis_Dibit(79)		L4	RC(6)	PC(3)	R41	Trellis_Dibit(25)	
L47	Trellis_Dibit(78)		L3	RC(5)	PC(2)	R42	Trellis_Dibit(24)	
L46	Trellis_Dibit(77)		L2	RC(4)	PC(1)	R43	Trellis_Dibit(23)	
L45	Trellis_Dibit(76)		L1	RC(3)	PC(0)	R44	Trellis_Dibit(22)	
L44	Trellis_Dibit(75)		R1	RC(2)	PC(15)	R45	Trellis_Dibit(21)	
L43	Trellis_Dibit(74)		R2	RC(1)	PC(14)	R46	Trellis_Dibit(20)	
L42	Trellis_Dibit(73)		R3	RC(0)	PC(13)	R47	Trellis_Dibit(19)	
L41	Trellis_Dibit(72)		R4	H1(4)	PC(12)	R48	Trellis_Dibit(18)	
L40	Trellis_Dibit(71)		R5	H1(3)	PC(11)	R49	Trellis_Dibit(17)	
L39	Trellis_Dibit(70)		R6	H1(2)	PC(10)	R50	Trellis_Dibit(16)	
L38	Trellis_Dibit(69)		R7	H1(1)	PC(9)	R51	Trellis_Dibit(15)	
L37	Trellis_Dibit(68)		R8	H1(0)	PC(8)	R52	Trellis_Dibit(14)	
L36	Trellis_Dibit(67)		R9	QR(7)	QR(6)	R53	Trellis_Dibit(13)	
L35	Trellis_Dibit(66)		R10	QR(5)	QR(4)	R54	Trellis_Dibit(12)	
L34	Trellis_Dibit(65)		R11	QR(3)	QR(2)	R55	Trellis_Dibit(11)	
L33	Trellis_Dibit(64)		R12	QR(1)	QR(0)	R56	Trellis_Dibit(10)	
L32	Trellis_Dibit(63)		R13	Golay(9)	Golay(8)	R57	Trellis_Dibit(9)	
L31	Trellis_Dibit(62)		R14	Golay(7)	Golay(6)	R58	Trellis_Dibit(8)	
L30	Trellis_Dibit(61)		R15	Golay(5)	Golay(4)	R59	Trellis_Dibit(7)	
L29	Trellis_Dibit(60)		R16	Golay(3)	Golay(2)	R60	Trellis_Dibit(6)	
L28	Trellis_Dibit(59)		R17	Golay(1)	Golay(0)	R61	Trellis_Dibit(5)	
L27	Trellis_Dibit(58)		R18	Trellis_Dibit(48)		R62	Trellis_Dibit(4)	
L26	Trellis_Dibit(57)		R19	Trellis_Dibit(47)		R63	Trellis_Dibit(3)	
L25	Trellis_Dibit(56)		R20	Trellis_Dibit(46)		R64	Trellis_Dibit(2)	
L24	Trellis_Dibit(55)		R21	Trellis_Dibit(45)		R65	Trellis_Dibit(1)	
L23	Trellis_Dibit(54)		R22	Trellis_Dibit(44)		R66	Trellis_Dibit(0)	

Table E.5: Transmit bit order for voice burst with SYNC (burst A)

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	V_Sync(47)	V_Sync(46)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	V_Sync(45)	V_Sync(44)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	V_Sync(43)	V_Sync(42)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	V_Sync(41)	V_Sync(40)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	V_Sync(39)	V_Sync(38)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	V_Sync(37)	V_Sync(36)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	V_Sync(35)	V_Sync(34)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	V_Sync(33)	V_Sync(32)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	V_Sync(31)	V_Sync(30)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	V_Sync(29)	V_Sync(28)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	V_Sync(27)	V_Sync(26)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	V_Sync(25)	V_Sync(24)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	V_Sync(23)	V_Sync(22)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	V_Sync(21)	V_Sync(20)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	V_Sync(19)	V_Sync(18)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	V_Sync(17)	V_Sync(16)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	V_Sync(15)	V_Sync(14)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	V_Sync(13)	V_Sync(12)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	V_Sync(11)	V_Sync(10)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	V_Sync(9)	V_Sync(8)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	V_Sync(7)	V_Sync(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	V_Sync(5)	V_Sync(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	V_Sync(3)	V_Sync(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	V_Sync(1)	V_Sync(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.6: Transmit bit order for voice burst with embedded signalling fragment 1

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	CC(3)	CC(2)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	CC(1)	CC(0)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	PI	LCSS(1)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	LCSS(0)	QR(8)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	LC(71)	LC(60)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	LC(49)	LC(39)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	LC(29)	LC(19)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	LC(9)	PC(15)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	LC(70)	LC(59)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	LC(48)	LC(38)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	LC(28)	LC(18)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	LC(8)	PC(14)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	LC(69)	LC(58)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	LC(47)	LC(37)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	LC(27)	LC(17)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	LC(7)	PC(13)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	LC(68)	LC(57)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	LC(46)	LC(36)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	LC(26)	LC(16)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	LC(6)	PC(12)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	QR(7)	QR(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	QR(5)	QR(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	QR(3)	QR(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	QR(1)	QR(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.7: Transmit bit order for voice burst with embedded signalling fragment 2

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	CC(3)	CC(2)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	CC(1)	CC(0)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	PI	LCSS(1)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	LCSS(0)	QR(8)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	LC(67)	LC(56)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	LC(45)	LC(35)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	LC(25)	LC(15)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	LC(5)	PC(11)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	LC(66)	LC(55)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	LC(44)	LC(34)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	LC(24)	LC(14)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	LC(4)	PC(10)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	LC(65)	LC(54)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	LC(43)	LC(33)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	LC(23)	LC(13)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	LC(3)	PC(9)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	LC(64)	LC(53)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	LC(42)	LC(32)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	LC(22)	LC(12)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	LC(2)	PC(8)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	QR(7)	QR(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	QR(5)	QR(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	QR(3)	QR(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	QR(1)	QR(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.8: Transmit bit order for voice burst with embedded signalling fragment 3

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	CC(3)	CC(2)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	CC(1)	CC(0)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	PI	LCSS(1)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	LCSS(0)	QR(8)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	LC(63)	LC(52)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	LC(41)	LC(31)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	LC(21)	LC(11)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	LC(1)	PC(7)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	LC(62)	LC(51)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	LC(40)	LC(30)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	LC(20)	LC(10)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	LC(0)	PC(6)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	LC(61)	LC(50)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	CS(4)	CS(3)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	CS(2)	CS(1)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	CS(0)	PC(5)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	H1(4)	H2(4)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	H3(4)	H4(4)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	H5(4)	H6(4)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	H7(4)	PC(4)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	QR(7)	QR(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	QR(5)	QR(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	QR(3)	QR(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	QR(1)	QR(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.9: Transmit bit order for voice burst with embedded signalling fragment 4

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	CC(3)	CC(2)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	CC(1)	CC(0)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	PI	LCSS(1)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	LCSS(0)	QR(8)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	H1(3)	H2(3)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	H3(3)	H4(3)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	H5(3)	H6(3)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	H7(3)	PC(3)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	H1(2)	H2(2)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	H3(2)	H4(2)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	H5(2)	H6(2)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	H7(2)	PC(2)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	H1(1)	H2(1)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	H3(1)	H4(1)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	H5(1)	H6(1)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	H7(1)	PC(1)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	H1(0)	H2(0)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	H3(0)	H4(0)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	H5(0)	H6(0)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	H7(0)	PC(0)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	QR(7)	QR(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	QR(5)	QR(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	QR(3)	QR(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	QR(1)	QR(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.10: Transmit bit order for voice burst with embedded RC

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	CC(3)	CC(2)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	CC(1)	CC(0)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	PI	LCSS(1)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	LCSS(0)	QR(8)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	RC(10)	PC(7)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	RC(9)	PC(6)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	RC(8)	PC(5)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	RC(7)	PC(4)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	RC(6)	PC(3)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	RC(5)	PC(2)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	RC(4)	PC(1)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	RC(3)	PC(0)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	RC(2)	PC(15)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	RC(1)	PC(14)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	RC(0)	PC(13)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	H1(4)	PC(12)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	H1(3)	PC(11)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	H1(2)	PC(10)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	H1(1)	PC(9)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	H1(0)	PC(8)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	QR(7)	QR(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	QR(5)	QR(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	QR(3)	QR(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	QR(1)	QR(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.11: Transmit bit order for voice burst with Null embedded message

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L66	VS(215)	VS(214)	L22	VS(127)	VS(126)	R23	VS(87)	VS(86)
L65	VS(213)	VS(212)	L21	VS(125)	VS(124)	R24	VS(85)	VS(84)
L64	VS(211)	VS(210)	L20	VS(123)	VS(122)	R25	VS(83)	VS(82)
L63	VS(209)	VS(208)	L19	VS(121)	VS(120)	R26	VS(81)	VS(80)
L62	VS(207)	VS(206)	L18	VS(119)	VS(118)	R27	VS(79)	VS(78)
L61	VS(205)	VS(204)	L17	VS(117)	VS(116)	R28	VS(77)	VS(76)
L60	VS(203)	VS(202)	L16	VS(115)	VS(114)	R29	VS(75)	VS(74)
L59	VS(201)	VS(200)	L15	VS(113)	VS(112)	R30	VS(73)	VS(72)
L58	VS(199)	VS(198)	L14	VS(111)	VS(110)	R31	VS(71)	VS(70)
L57	VS(197)	VS(196)	L13	VS(109)	VS(108)	R32	VS(69)	VS(68)
L56	VS(195)	VS(194)	L12	CC(3)	CC(2)	R33	VS(67)	VS(66)
L55	VS(193)	VS(192)	L11	CC(1)	CC(0)	R34	VS(65)	VS(64)
L54	VS(191)	VS(190)	L10	PI	LCSS(1)	R35	VS(63)	VS(62)
L53	VS(189)	VS(188)	L9	LCSS(0)	QR(8)	R36	VS(61)	VS(60)
L52	VS(187)	VS(186)	L8	N_LC(10)	PC(7)	R37	VS(59)	VS(58)
L51	VS(185)	VS(184)	L7	N_LC(9)	PC(6)	R38	VS(57)	VS(56)
L50	VS(183)	VS(182)	L6	N_LC(8)	PC(5)	R39	VS(55)	VS(54)
L49	VS(181)	VS(180)	L5	N_LC(7)	PC(4)	R40	VS(53)	VS(52)
L48	VS(179)	VS(178)	L4	N_LC(6)	PC(3)	R41	VS(51)	VS(50)
L47	VS(177)	VS(176)	L3	N_LC(5)	PC(2)	R42	VS(49)	VS(48)
L46	VS(175)	VS(174)	L2	N_LC(4)	PC(1)	R43	VS(47)	VS(46)
L45	VS(173)	VS(172)	L1	N_LC(3)	PC(0)	R44	VS(45)	VS(44)
L44	VS(171)	VS(170)	R1	N_LC(2)	PC(15)	R45	VS(43)	VS(42)
L43	VS(169)	VS(168)	R2	N_LC(1)	PC(14)	R46	VS(41)	VS(40)
L42	VS(167)	VS(166)	R3	N_LC(0)	PC(13)	R47	VS(39)	VS(38)
L41	VS(165)	VS(164)	R4	H1(4)	PC(12)	R48	VS(37)	VS(36)
L40	VS(163)	VS(162)	R5	H1(3)	PC(11)	R49	VS(35)	VS(34)
L39	VS(161)	VS(160)	R6	H1(2)	PC(10)	R50	VS(33)	VS(32)
L38	VS(159)	VS(158)	R7	H1(1)	PC(9)	R51	VS(31)	VS(30)
L37	VS(157)	VS(156)	R8	H1(0)	PC(8)	R52	VS(29)	VS(28)
L36	VS(155)	VS(154)	R9	QR(7)	QR(6)	R53	VS(27)	VS(26)
L35	VS(153)	VS(152)	R10	QR(5)	QR(4)	R54	VS(25)	VS(24)
L34	VS(151)	VS(150)	R11	QR(3)	QR(2)	R55	VS(23)	VS(22)
L33	VS(149)	VS(148)	R12	QR(1)	QR(0)	R56	VS(21)	VS(20)
L32	VS(147)	VS(146)	R13	VS(107)	VS(106)	R57	VS(19)	VS(18)
L31	VS(145)	VS(144)	R14	VS(105)	VS(104)	R58	VS(17)	VS(16)
L30	VS(143)	VS(142)	R15	VS(103)	VS(102)	R59	VS(15)	VS(14)
L29	VS(141)	VS(140)	R16	VS(101)	VS(100)	R60	VS(13)	VS(12)
L28	VS(139)	VS(138)	R17	VS(99)	VS(98)	R61	VS(11)	VS(10)
L27	VS(137)	VS(136)	R18	VS(97)	VS(96)	R62	VS(9)	VS(8)
L26	VS(135)	VS(134)	R19	VS(95)	VS(94)	R63	VS(7)	VS(6)
L25	VS(133)	VS(132)	R20	VS(93)	VS(92)	R64	VS(5)	VS(4)
L24	VS(131)	VS(130)	R21	VS(91)	VS(90)	R65	VS(3)	VS(2)
L23	VS(129)	VS(128)	R22	VS(89)	VS(88)	R66	VS(1)	VS(0)

Table E.12: Transmit bit order for standalone RC burst

Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0	Symbol	Bit 1	Bit 0
L24	CC(3)	CC(2)	L8	R_Sync(39)	R_Sync(38)	R9	R_Sync(7)	R_Sync(6)
L23	CC(1)	CC(0)	L7	R_Sync(37)	R_Sync(36)	R10	R_Sync(5)	R_Sync(4)
L22	PI	LCSS(1)	L6	R_Sync(35)	R_Sync(34)	R11	R_Sync(3)	R_Sync(2)
L21	LCSS(0)	QR(8)	L5	R_Sync(33)	R_Sync(32)	R12	R_Sync(1)	R_Sync(0)
L20	RC(10)	PC(7)	L4	R_Sync(31)	R_Sync(30)	R13	RC(2)	PC(15)
L19	RC(9)	PC(6)	L3	R_Sync(29)	R_Sync(28)	R14	RC(1)	PC(14)
L18	RC(8)	PC(5)	L2	R_Sync(27)	R_Sync(26)	R15	RC(0)	PC(13)
L17	RC(7)	PC(4)	L1	R_Sync(25)	R_Sync(24)	R16	H1(4)	PC(12)
L16	RC(6)	PC(3)	R1	R_Sync(23)	R_Sync(22)	R17	H1(3)	PC(11)
L15	RC(5)	PC(2)	R2	R_Sync(21)	R_Sync(20)	R18	H1(2)	PC(10)
L14	RC(4)	PC(1)	R3	R_Sync(19)	R_Sync(18)	R19	H1(1)	PC(9)
L13	RC(3)	PC(0)	R4	R_Sync(17)	R_Sync(16)	R20	H1(0)	PC(8)
L12	R_Sync(47)	R_Sync(46)	R5	R_Sync(15)	R_Sync(14)	R21	QR(7)	QR(6)
L11	R_Sync(45)	R_Sync(44)	R6	R_Sync(13)	R_Sync(12)	R22	QR(5)	QR(4)
L10	R_Sync(43)	R_Sync(42)	R7	R_Sync(11)	R_Sync(10)	R23	QR(3)	QR(2)
L9	R_Sync(41)	R_Sync(40)	R8	R_Sync(9)	R_Sync(8)	R24	QR(1)	QR(0)

Annex F (normative): Timers and constants in DMR

F.0 Timers and constants in DMR - Introduction

This annex lists the timers and constants in a DMR entity.

Where indicated, a value should be chosen by the MS/BS designer from within the specified range. For other timers and constants, a default value may be specified and the value of these timers and constants shall be configurable within the DMR entity (MS or BS).

F.1 Layer 2 timers

T_ChMonTo Channel activity monitoring time-out.
Minimum value = 40 ms.

T_ChSyncTo Channel activity synchronization time-out.
Minimum value = 390 ms.

T_MSInactiv MS inactivity timer.
Default value = 5 s.
Maximum value = infinite.

T_CallHt Call hangtime period.
Default value = 3 s.
Maximum value = infinite.

T_ChHt Channel hangtime period.
T_ChHt = T_MSInactiv - T_CallHt.

T_Monitor Monitor timer.
Value chosen by MS designer.
Maximum value = 720 ms.

NOTE 1: The Monitor timer is the duration of time an MS has been monitoring the channel for RF and attempting to acquire synchronization.

T_TxCC TX CC timer.
Value chosen by MS designer.
Maximum value = 360 ms.

NOTE 2: The TX CC timer is a direct mode only timer. It is used when a transmission is requested from the Out_of_Sync or In_Sync_Unknown_System states and the MS has determined activity resides on the channel. This timer sets the duration that the MS will attempt to acquire the Colour Code information embedded in the received DMR signal.

T_SyncWu Sync WU timer.
Value chosen by MS designer.
Maximum value = 360 ms.

NOTE 3: The Sync WU timer is a MS mode parameter. This timer sets the duration that the MS will attempt to acquire a DMR sync pattern after transmission of the Wakeup PDU to activate the BS outbound.

T_TxCCSlot TX CC slot timer.
Value chosen by MS designer.
Maximum value = 720 ms.

NOTE 4: The TX CC slot timer is a MS mode timer. It is used when a transmission is requested from the Out_of_Sync or In_Sync_Unknown_System states and the MS has determined activity resides on the channel. This timer sets the duration that the MS will attempt to acquire the Colour Code and slot numbering information embedded in the received DMR signal.

T_IdleSrch Idle Search timer.
Value chosen by MS designer.
Maximum value = 540 ms.

NOTE 5: The Idle Search timer is a MS mode timer. It is used when a transmission is requested and the MS has matched the Colour Code and determined the slotting structure. This timer sets the duration that the MS will attempt to determine the desired slot is idle before denying the transmission.

T_Holdoff Random holdoff timer.
Range chosen by MS designer.
MS randomly generates timer duration from uniform distribution over the range.
Minimum value = 0 ms.
Recommended maximum value = 1 000 ms for non-time critical CSBK ACK/NACK messages.

NOTE 6: The Random_Holdoff_Timer is a MS mode timer. It is used when a non-time critical transmission is required and the channel is busy. Here the MS waits a random amount of time before attempting to transmit again. The actual range will be application specific.

NOTE 7: A use case example is data messages that are queued while the MS is waiting for the channel to become idle. This will reduce collisions at the BS.

F.2 Layer 2 constants

N_RssiLo RSSI threshold value for monitoring channel activity.
Recommended default values for Polite to All channel access policy are shown in table F.1.
Recommended default value for Polite to Own Colour Code channel access policy is -122 dBm.
The absolute accuracy shall not exceed ±4 dB.

Table F.1: Recommended default Polite to All N_RssiLo threshold levels

Frequency band	Default threshold level (dBm)
50 MHz to 137 MHz	-101
> 137 MHz to 300 MHz	-107
> 300 MHz	-113
NOTE: The threshold levels are given for a 50 Ω impedance.	

N_Wakeup Wakeup Message Threshold.
Value chosen by MS designer.
Suggested value = 2

NOTE 1: The Wakeup Message Threshold is a MS mode parameter. It sets the maximum number of times an MS will loop through the TX_Wakeup state while attempting to activate the BS outbound.

n_DFragMax Data fragment maximum length.
Value = 1 500 octets.

NOTE 2: Protocol layer 2 needs to buffer up to N_DFMax data length before passing to higher layer.

N_BlockMax Maximum number of blocks in a packet, including the header block.

Annex G (informative): High level states overview

G.0 High level states overview - Introduction

This annex describes some SDL diagrams which may be used as an overview of high level states. As this annex is informative, real implementations may have different state descriptions.

G.1 High Level MS states and SDL description

G.1.0 General

High Level MS states are divided into two levels. The first level deals with synchronization, Colour Code (CC) and slotting (repeater mode and TDMA direct mode only) recognition. The second level deals with general hangtime, reception and transmission control.

NOTE: These levels will be referenced for various facilities in ETSI TS 102 361-2 [5] as well as for channel access.

G.1.1 MS Level 1 SDL

The MS Level 1 SDLs are shown in figure G.1 for direct mode, figure G.2 for repeater mode and figure G.3 for TDMA direct mode respectively. The Level 1 states are Out_of_Sync and In_Sync. These are defined below:

- **Out_of_Sync:** This state occurs when the MS has not acquired or has lost sync on the channel. This can occur due to numerous reasons, stemming from lack of signal or co-channel interference from analogue or digital radios to travelling through a deep fade.
- **In_Sync:** This state occurs after a MS has successfully detected DMR voice or data sync. In this state the MS searches for matching Colour Code in direct mode and matching Colour Code and outbound slotting structure in repeater mode.

The In_Sync state is further divided into 2 levels. These are Unknown_System and My_System. Descriptions of these states are listed below.

- **Unknown_System:** This state occurs when the Colour Code in direct mode or both the Colour Code and slot number identifier in repeater mode or TDMA direct mode are unknown to the receiver MS. If the Colour Code does not match or sync is lost, the MS transitions to the Out_of_Sync state. If the Colour Code matches and the slotting structure is determined (repeater mode only) the MS transitions to the My_System state.
- **My_System:** This state occurs when the Colour Code in direct mode or both the Colour Code and slot number identifier in repeater mode are known to the receiver MS. If sync is lost or the Colour Code can no longer be decoded, the MS transitions to the Out_of_Sync state. It will also transition to the Out_of_Sync state when it loses confidence in the Colour Code.

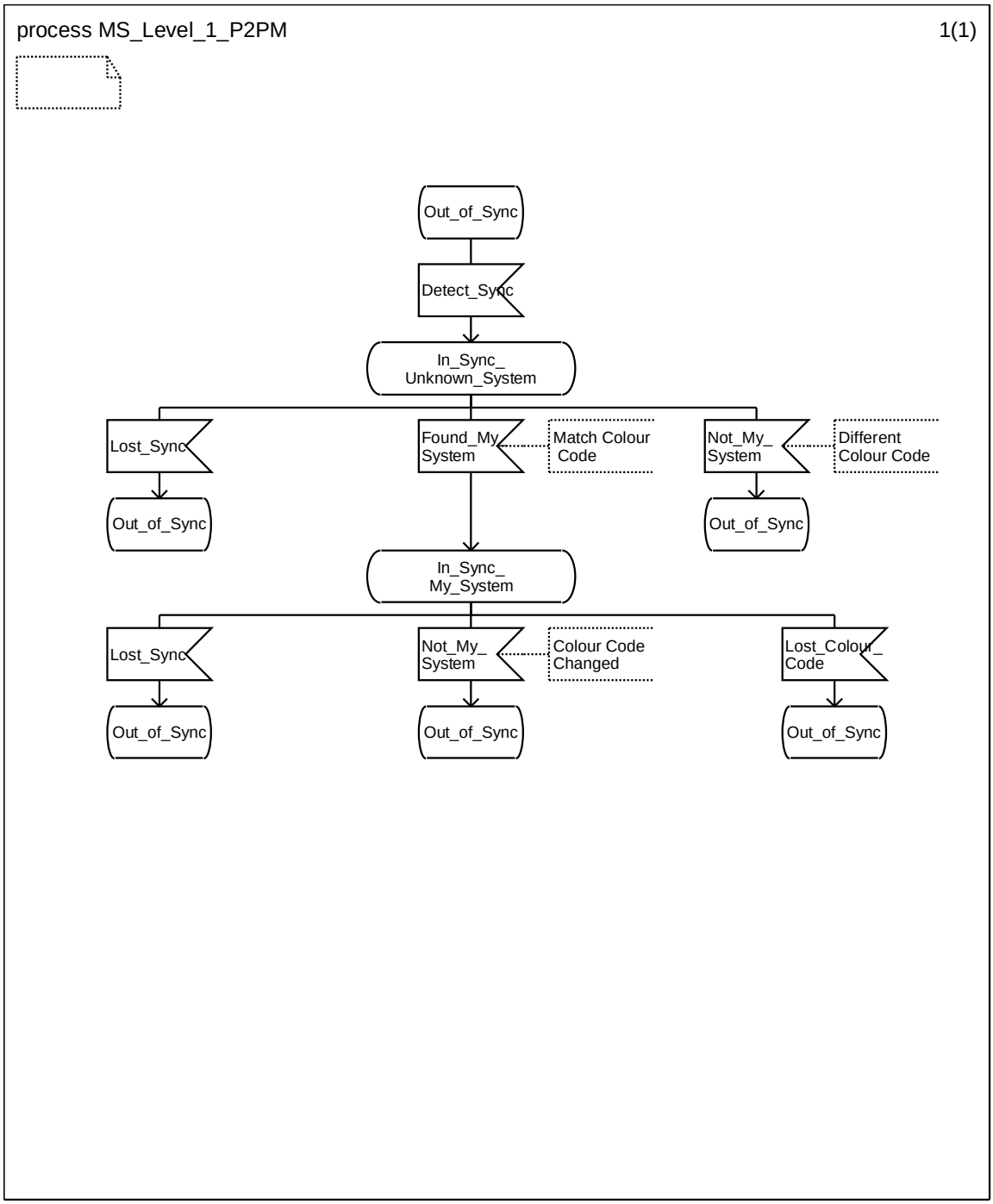


Figure G.1: MS Level 1 SDL: direct mode

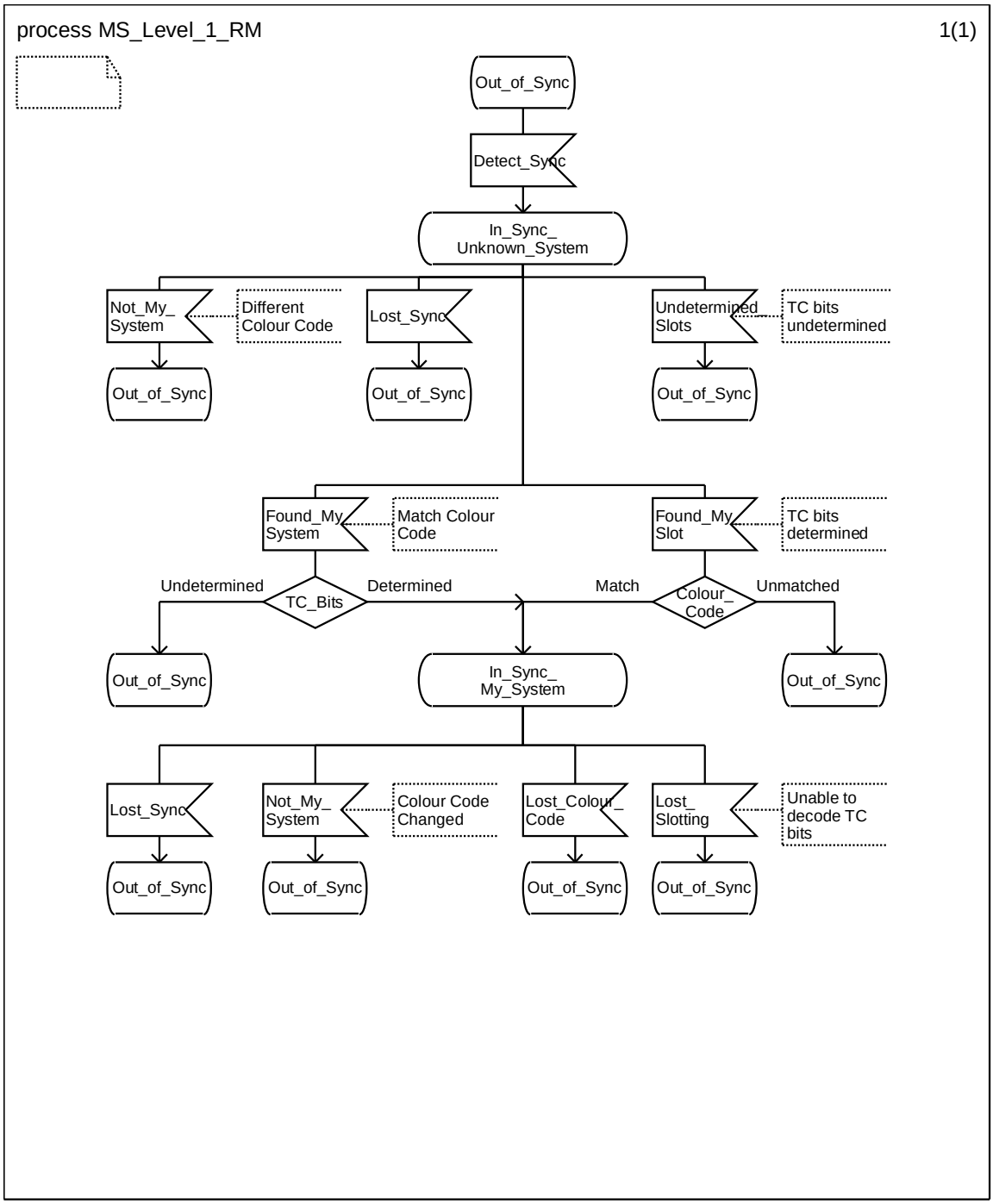


Figure G.2: MS Level 1 SDL: repeater mode

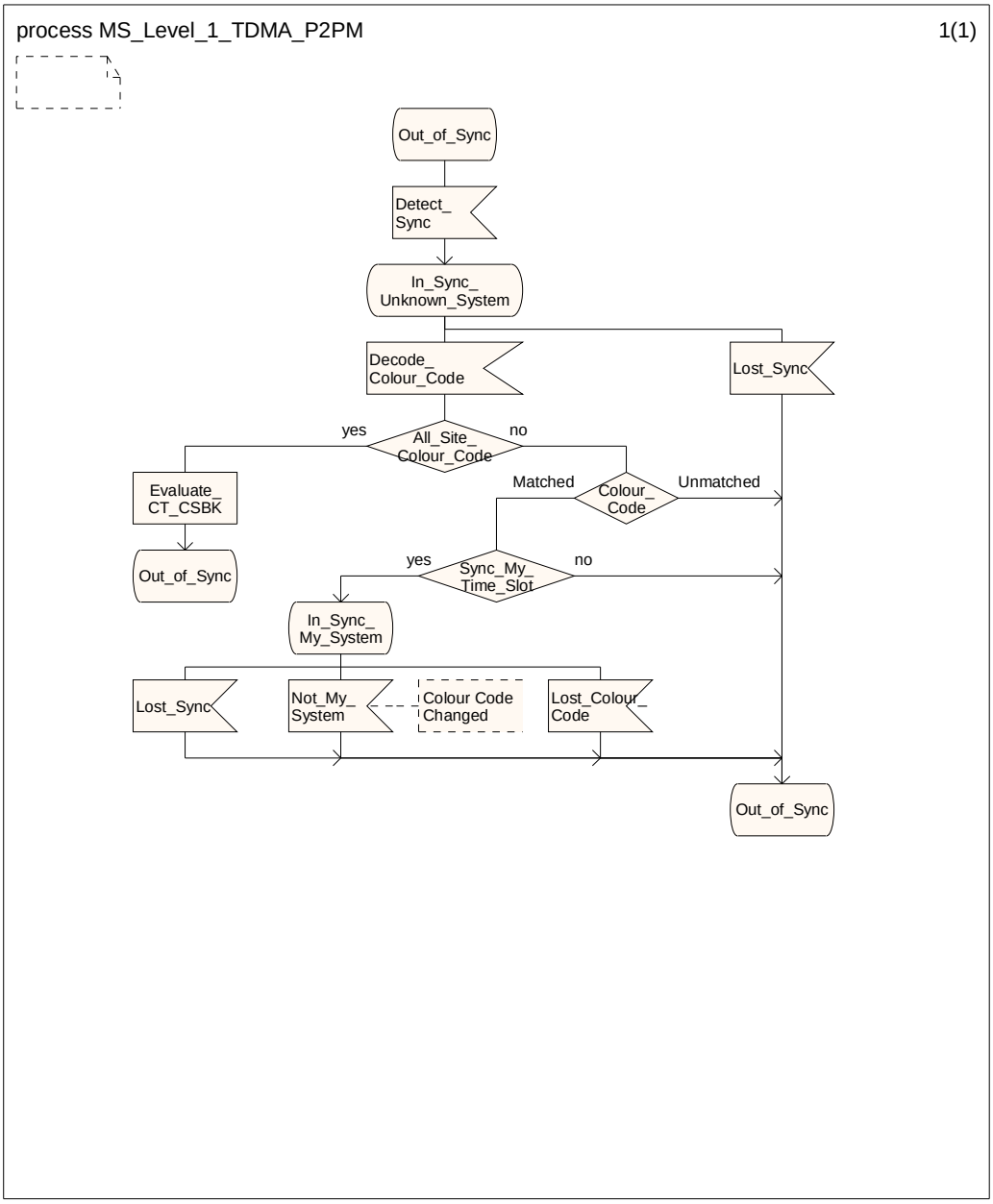


Figure G.3: MS Level 1 SDL: TDMA direct mode

G.1.2 MS Level 2 SDL

The MS Level 2 SDL occurs in the Level 1 In_Sync_My_System state. These are the same for direct mode, repeater mode and TDMA direct mode and are illustrated in figure G.4. The Level 2 states are Not_in_Call, My_Call, Others_Call, In_Session and Transmit. These are defined below:

NOTE 1: Group Call HMSC and MSCs reference these states.

- **Not_in_Call:** An MS resides in this state when it is unable to determine a destination ID. In repeater mode this can occur during channel hangtime. Determination of a destination ID transitions the MS to either My_Call, Others_Call or In_Session state.

- **My_Call:** In this state the MS talk group(s) or individual ID is decoded during voice traffic via a Voice_LC_Header or an Embedded_LC. Here the MS is party to the call.

- **Others_Call:** An MS transitions to this state when the received talk group(s) or individual ID does not match the talk group(s) or individual ID of the MS. While in this state if a new ID matches, then it will transition to either My_Call if received via a Voice_LC_Header or an Embedded_LC or In_Session if received via a Voice_Terminator_with_LC.

NOTE 2: This state includes the reception of both voice and call hangtime for the other call.

- **In_Session:** An MS transitions to this state when the MS talk group(s) or individual ID is decoded via a Voice_Terminator_with_LC. This is call hangtimeHere the MS is party to the call.

- **Transmit:** In this state the MS transmits voice, data or CSBKs in the appropriate slot.

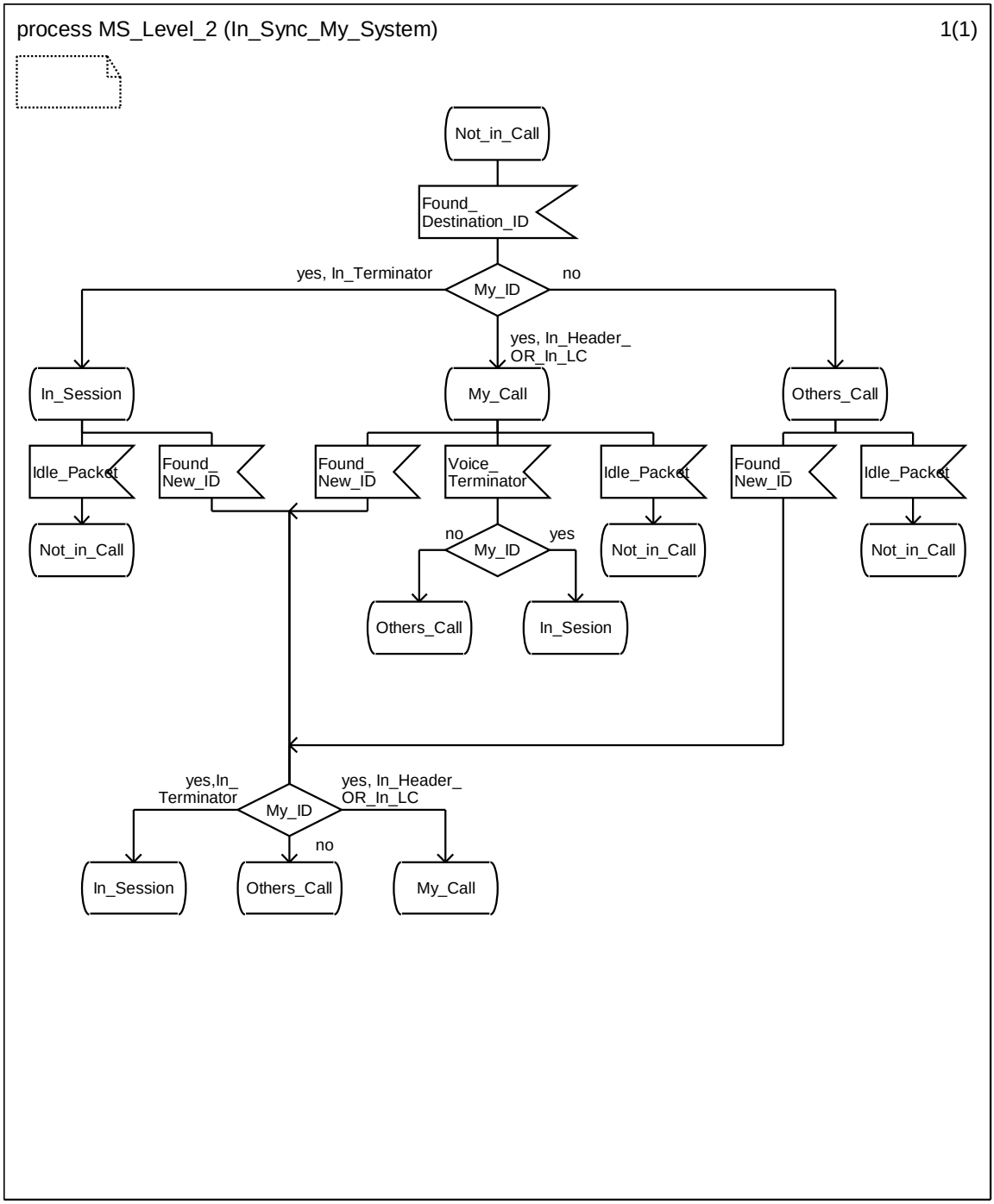


Figure G.4: MS level 2 SDL

G.2 High level BS states and SDL descriptions

G.2.0 High level BS states and SDL descriptions - Introduction

High Level BS states are divided into two levels. The first level deals with the control of both slots and activating and deactivating the BS outbound channel. The second level deals with control of a single slot. This level describes repeating, call hangtime and channel hangtime.

In the figures G.5 and G.6 the slot number refers to the outbound slot. Therefore, outbound slot 1 implies inbound slot 1 for offset mode and inbound slot 2 for aligned mode, as defined in clause 5.1 of the present document. Also in figures G.5 and G.6, BOR and EOR are events that cause High Level BS transitions. These are overview conceptual messages that will be feature specific.

G.2.1 BS Both Slots SDL

The BS Both Slots SDL describes the overall control of both slots and is illustrated in figure G.5. The states are BR_Hibernating, Hangtime, Repeating_Slot_1, Repeating_Slot_2 and Repeating_Both_Slots. These states are defined below:

- **BS_Hibernating:** In this state the BS is attempting to decode a valid wakeup message from an MS. The outbound is inactive during this state. Upon reception of a valid wakeup message the BS starts a Mobile Station Inactivity Timer (T_MSInactiv) and transitions to the Hangtime state.

NOTE: The T_MSInactiv is a timer that starts when no valid activity is detected on the inbound channel or upon the reception of a valid wakeup message. Reception of valid activity with the exception of the wakeup message cancels the T_MSInactiv.

- **Hangtime:** In this state the BS is transmitting channel hangtime (Idle) messages on both slots. The reception of bursts will transition the BS to the appropriate repeating state; Repeating_Slot_1 or Repeating_Slot_2. Also, the expiration of the T_MSInactiv will transition the BS back to the BR_Hibernating state.

- **Repeating_Slot_1:** In this state the BS is actively repeating bursts on slot 1 and transmitting Idle messages on slot 2. An EOR_Slot_1 will transition the BS to the Hangtime state. A BOR_Slot_2 will transition the BS to the Repeating_Both_Slots state.

- **Repeating_Slot_2:** In this state the BS is actively repeating bursts on slot 2 and transmitting Idle messages on slot 1. An EOR_Slot_2 will transition the BS to the Hangtime state. A BOR_Slot_1 will transition the BS to the Repeating_Both_Slots state.

- **Repeating_Both_Slots:** In this state the BS is repeating activity on both slots. An EOR_Slot_1 or EOR_Slot_2 will transition the BS to the respective Repeating_Slot_1 or Repeating_Slot_2 states.

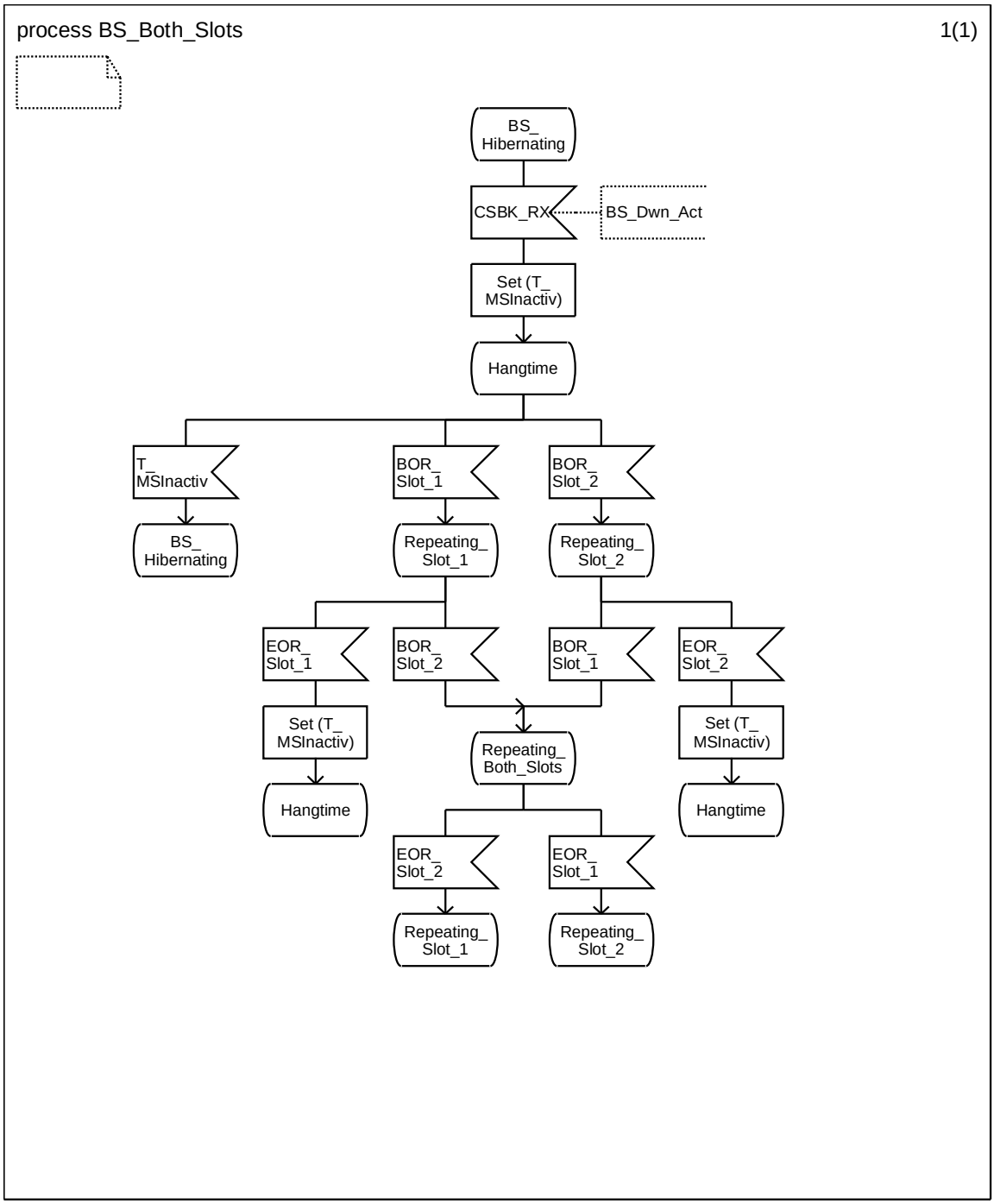


Figure G.5: BS Both Slots SDL

G.2.2 BS Single Slot SDL

The BS Single Slot SDL describes the overall control of one of the two TDMA slots and is illustrated in figure G.6. The states are Channel_Hangtime, Call_Hangtime, and Repeating_Slot. These states are defined below:

- **Channel_Hangtime:** In this state the BS is transmitting channel hangtime (Idle) messages on the slot. The reception of bursts will transition the BS to the Repeating_Slot state.
- **Call_Hangtime:** In this state the BS is transmitting call hangtime (Voice_Terminator_with_LC) messages on the slot. The reception of bursts will transition the BS to the Repeating_Slot state. Also, the expiration of call hangtime transitions the BS slot to the Channel_Hangtime state.

- **Repeating_Slot:** In this state the BS is actively repeating bursts on the slot. An EOR will transition the BS to the Call_Hangtime state.

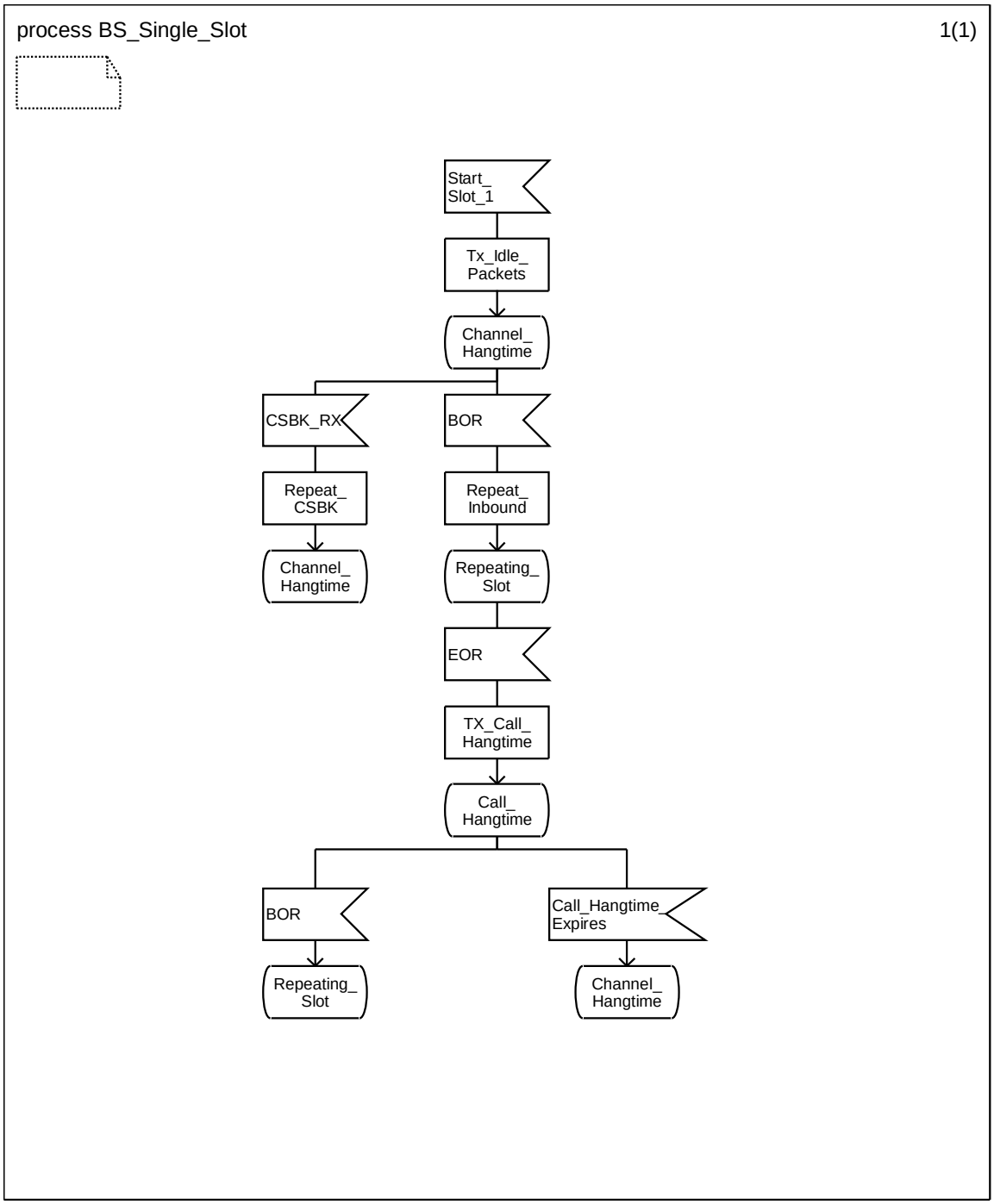


Figure G.6: BS Single Slot SDL

Annex H (normative): Feature interoperability

H.0 Feature interoperability - Introduction

The FID identifies one of several different feature sets.

The FLCO identifies the "over-air" feature within the given feature set.

To ensure interoperability at the air interface, features that are standardized in the Services and Facilities specification ETSI TS 102 361-2 [5] and available in the equipment shall be accessible only via the combination of default SFID and corresponding FLCO.

Features that are not standardized in the Services and Facilities specification ETSI TS 102 361-2 [5] are only available via an alternative MFID.

H.1 Feature set ID (FID)

Each manufacturer may have multiple values of the MFIDs. The same MFID may be used for various protocols or products if suitable from the manufacturer's point of view.

It is allowed that multiple manufacturers or application designers use the same MFID.

There is one range on FIDs available for MFID specific allocation as defined in clause 9.3.13 and copied in a short form into table H.1.

Table H.1: Feature set ID information element content

Information element	Length	Value	Remark
Feature set ID	8	00000000_2	Standardized feature set ID for the services and facilities defined in ETSI TS 102 361-2 [5] (SFID)
		00000001_2	Reserved for future standardization
		00000010_2	Reserved for future standardization
		00000011_2	Reserved for future standardization
		00000100_2	Manufacturer's specific feature set ID (MFID)
		etc.	etc.
		01111111_2	Manufacturer's specific feature set ID (MFID)
		$1xxxxxxx_2$	Reserved for future MFID's allocation (MFID)

H.2 Application for Manufacturer's Feature set ID

This application form is provided by ETSI who is the central body for the management of the Manufacturer's Feature set ID (MFID) values as described in the present document, clause 9.3.13. The application and allocation may be implemented by other means such as a World Wide Web server application.

This form presented in annex I may be changed without notice by ETSI.

Annex I (informative): Void

Annex J (informative): Change requests

The present document contains change requests as described in table J.1.

Table J.1: Change requests

No	Standard Version	Clauses affected or description	Title
001	1.1.1	B.2.1, B.2.3	Clarification for BPTC parity calculation
002	1.1.1	7.2, 9.1.8, 9.3.31and addition of 7.4	Add MBC message structure to Part 1 of standard for document consistency
003	1.1.1	8.2.2.1, 8.2.2.2, 9.2.1, 9.2.2, 9.2.3, 9.2.4, 9.2.5, 9.2.6, 9.2.7, 9.2.8, 9.3.6, 9.3.22	Change data slot types of confirmed and unconfirmed data to ½ rate and ¾ rate coding
004	1.1.1	New clauses 8.2.1.5, 8.2.1.6, 8.2.1.7, 9.2.10, 9.2.11, 9.2.12, 9.3.33, 9.3.34, 9.3.35, 9.3.36, 9.3.37, 9.3.38	Add short data header block structure to Part 1 of standard for document consistency
005	1.1.1	6.2 table 6.1	Table 6.1 has to be updated according the changes of CR002 and CR003
006	1.1.1	Annex B table B.1	Table B.1 has to be updated according the changes of CR002 and CR003
007	1.1.1	9.3.18	SAP identifier values need to be updated due to data resolutions
008	1.1.1	9.3.17	Data Format values need to be updated due to CR004 and CR009
009	1.1.1	New clauses 8.2.1.8, 8.2.2.5, 9.2.13, 9.2.14, 9.3.39, 9.3.40, 9.3.41, 9.3.42	UDT message structure need to be added to Part 1 of standard for document consistency
010	1.2.1	8.2.1.1, 8.2.1.2, 9.2.1, 9.2.6, new 9.3.17A, 9.3.18	IP header compression
011	1.2.1	1, 3.1, 3.3, 4, 4.1	Clarifications and editorial modifications
012	1.2.1	4.2.1, 4.3, 4.61, 5.1.2.2, 5.1.2.3, 5.1.3.1, 5.1.4.5, 5.1.5.2, 5.1.5.4, 5.1.2.7, 5.2.2, 5.2.2.1, 5.2.2.2, 5.2.2.2.1, 5.2.2.3	Modifications in clauses 4 and 5
013	1.2.1	6.1, 6.2, 6.3, 6.4.2, 7.1, 7.1.3, 7.1.3.2, 7.2, 7.3, 7.4	Modifications in clauses 6 and 7
014	1.2.1	8.1, 8.2, 8.2.1, 8.2.1.1 to 8.2.1.8, 8.2.2.1 to 8.2.2.5	Modifications in clause 8
015	1.2.1	9.1.4, 9.1.9, 9.2.9, 9.2.13, 9.3.5, 10.2.3.1.1 to 10.2.3.1.3, 10.2.3.2.1, 10.2.3.2.2	Modifications in clauses 9 and 10
016	1.2.1	Annex A, B, B.2.1, B.2.3, B.3.6, B.3.8, C.1, C.2, D, D.1, D.2, E, F.1, G.1, G.1.1, G.1.2	Modifications in annexes
017	1.3.1	7.1.1, 7.1.2, 7.2.1, 7.4.1, 8.2.1, 8.2.2.2, B.3.12	Addition of Slot Type CRC inversion mask to improve protocol robustness
018	1.3.1	Annex B, table B.1	Alignment of terminology of table 9.22 and table B.1
019	1.4.1	8.2.2.4	Align Data Terminator LC definition throughout documents
020	1.4.1	8.2.1	Correct Data Header CRC cross reference
021	1.4.1	7.1	Correct Short LC Figure
022	1.4.1	9.3.21, 9.3.33, 9.3.40 and 9.3.41	Data Blocks to Follow Information Element
023	1.4.1	B.3.7, B.3.8, B.3.9 and B.3.10 and 3.3	CRC clarification to reduce ambiguity
024	1.4.1	B.1.1and E table E.1 and E.2	BPTC (196,96) Performance Improvement
025	1.4.1	Annex E table E.4	Table E.4 Correction
026	1.4.1	8.2.1.3, 9.2.1, 9.2.4, 9.2.5, 9.2.6, 9.2.11, 9.2.12 and 9.3.20	Response Data header correction
027	1.4.1	Annex B table B.1	Table B.1 correction
028	1.4.1	B.1.1, B.2.4	Rate ½ and Rate ¾ editorial changes
029	1.4.1	6.1	Vocoder Socket Voice Frame order
030	1.4.1	8.2.2.1, 8.2.2.2, 9.2.2, 9.2.7	Confirmed and Unconfirmed Data
031	1.4.1	9.2.8, 9.2.14	Clause 8.3 reference removal
032	1.4.1	6.2, 9.3.6, B.3.12	Data type clarification
033	1.4.1	5.2.1.3	BS Activation clarification

No	Standard Version	Clauses affected or description	Title
034	1.4.1	6.2, 8.2, 8.2.2.1, 8.2.2.2, 9.2, 9.3.22, 9.3.6, B, B.2, B.3.12	Rate 1 Data transmission
035	1.4.1	8.2.1.3, 8.2.1.4, 8.2.1.5, 8.2.1.6, 8.2.1.7, 8.2.1.8, 9.2.1, 9.2.4, 9.2.6, 9.2.10, 9.2.11, 9.2.12, 9.2.13	DPF and Format alignment
036	1.4.1	F.1 and F.2	Layer 2 Timer and Constant Changes
037	1.4.1	9.2.8	Rate ½ Last Data Block Corrections
038	1.4.1	5.2.1.4, 5.2.2.1.1, 5.2.2.2.1, 5.2.2.2.4 and 7.3	Typo Changes
039	1.4.1	5.1.1.1 and 5.1.1.2	Slot Numbering Clarification
040	1.4.1	9.3.33	Appended Blocks Clarification Note
041	1.4.1	5.2.2.3	Impolite CSBK responses
042	1.4.1	8.1 and 9.3.25	Fragment Sequence Number Clarification
043	1.4.1	B.3.9	Rewording of part of CR023
044	1.4.4	5.2.1.6	Transmit admit criteria correction
045	1.4.4	8.2.2.3	Response packet definition table correction

History

Document history		
V1.1.1	April 2005	Publication
V1.2.1	January 2006	Publication
V1.3.1	September 2006	Publication
V1.4.1	December 2006	Publication
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V2.1.1	April 2012	Publication
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